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Impending Form Interpretations for Delay to Ramp and Step Input On-Chip VLSI RLC Annex

Vimal Kishore Yadav[1], Pratiksha Singh Gaur[2], Sucheta Yadav[3]

Assistant Professor, Dept. of Electronics and Communication Engineering, Amity University, Madhya Pradesh, India[1]

Dept. of Electronics and Communication Engineering, Amity University, Madhya Pradesh, India [2]

Assistant. Professor, Dept. of Electronics and Communication Engineering, G.L Bajaj, Mathura, India [3]

Abstract: In a high speed digital integrated circuit, annex delay can be momentous and hold for factual exploration by using moments of impulse response delay exploration has been done. Elmore delay is (the first moment of impulse response) interpretation, to moment matching approach which establish reduced order trans-impedance and transfer function approximations. The elmore delay is swift becoming inadequate for deep submicron technologies and reduced order transfer function delays are un-functional for use as early phase design matrices. This paper interpret access for fitting moments of the impulse response to probability density function, so that delay can be appraisal factually for RLC trees, it is a demonstrated that inverse gamma function provides a provable stable approximation. For prolong delay matrices for ramp inputs to the more general and realistic non-step input, we use PERI (probability distribution function extension for ramp input) technology. The factual model consequence compared with MATLAB simulation.

Keywords: Moment Matching, On-Chip Interconnect, Probability Distribution function, Cumulative Distribution function, Delay calculation, Slew Calculation, Beta Distribution, VLSI.

I. INTRODUCTION

There have been drastic changes in the design methodologies of integrated circuits and systems. The paradigm shift is one of the most important factors to determine the integrated circuit performance. There has been a continuous change in the feature sizes of the integrated circuits and are well scaled down below 0.18 microns. Because of some of the interconnect limitations the interconnect dimensions are scaled with the devices whenever possible. Nowadays IC's accommodate a large number of metallization layers and there are many more to come in the future. This paper generally proposes an extension to Elmore's approximation in order to match the higher order moments of the probability density function. A gamma function approximation is used with the RLC trees and the moments are fitted into the gamma function in order to characterize the gamma function. There is a possibility of some wire ability problem which may result due to the multilevel interconnects. Once the moments are fitted into the gamma function we can obtain the step response delay and the slew as a closed form expression thereby providing the same explicitness same as that of the Elmore's approximation.

II. BASIC THEORY-

II.I Moment of Linear Circuit Response

Let h (t) be a circuit impulse response in the time domain and let H(s) be the corresponding transfer function. By definition, H(s) is the Laplace transform of h (t) [12],

$$H(s) = \int_0^\infty h(t)e^{-st}dt \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Applying Taylor series

$$H(s) = \sum_0^\infty \frac{(-1)}{i} s^i \int_0^\infty s^i h(t)dt$$

Now apply different limits for finding m_o, m_1, m_2, m_3 ……. m_n

$$m_0 = \int_0^1 th(t)dt$$

$$m_0 = h(t)\int_0^1 tdt$$

After solving m_0 we get

$$m_0 = \frac{h(t)}{2}$$

Similarly,

$$m_1 = 2h(t)$$

$$m_2 = \frac{9h(t)}{2}$$

$m_3 = 8h(t)$ and so on…

Now transfer function h (t) can be expressed as,

$$H(s) = m_0 + m_1 s + m_2 s^2 + m_3 s^3 + \ldots\ldots$$

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$$H(s) = \frac{h(t)}{2} + 2h(t) + \frac{9h(t)}{2} + 8h(t) + \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

II.II Central moments-

We can used to explain the properties of elmore delay approximation by using Elmore's distribution function analogy. Central moments are the distribution theory concepts same as to moments.
Consider moment definition given,

$$p_q = \frac{(-1)^q}{q} \int_0^s q h(t) dt$$

This means impulse is given response by [9, 10]

$$\gamma = \frac{\int_0^\infty t h(t)}{\int_0^\infty h(t) dt} = -\frac{m_1}{m_0}$$

Few central moments can be expressed in terms of circuit moment [11]

$\gamma_0 = m_0$,

$\gamma_1 = 0$,

$$\gamma_2 = 2m_2 - \frac{m_1^2}{m_0}$$

$$\gamma_3 = -6m_3 + 6\frac{m_1 m_2}{m_0} - 2\frac{m_1^3}{m_0^2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

(γ_0) is the area under the curve, which is unity.

(γ_2) is the variance of the distribution function which measure spread of the curve from the centre.

(γ_3) is the measure of skew-ness of the distribution function.

III Proposed model

Elmore approximated the interconnect delay based on the analogy between non-negative impulse responses and Probability Distribution Function (PDF). In order to capture the RC interconnect delay various probability functions have been used with varying accuracy. The Beta distribution is a reasonably good representation of RC tree impulse responses since it provides good "coverage" of bell shaped curves which are bounded on the left and exponentially decaying to the right.

Beta distribution is given by[14]

$$B(p,q) = \int_0^1 v^{p-1}(1-v)^{q-1} dv \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

One can easily generate the PDF of Beta distribution by using Mat lab. Figure 1 given below is the Beeta distribution PDF with *P (a, b)* on y-axis and X on x-axis which is generated in Mat lab 7 for different values of constants *p* andq.

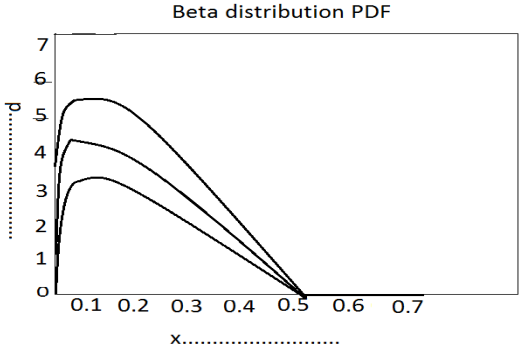

Fig.1. Beta distribution PDF for Different values of constants *p* and *q*

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III.I Calculation of the delay metrics-

(μ) is the mean,(σ_2)is the variance,(γ_3)is the skew-ness (σ_1)is the standard deviation

$$\mu = \frac{p}{p+q} \quad \ldots\ldots(6)$$

$$\sigma_2 = \frac{pq}{(p+q)^2(p+q+1)} = \frac{pq}{(p^2+q^2+2pq)(p+q+1)} \quad \ldots\ldots(7)$$

$$\gamma_3 = \frac{2(q-p)(p+q+1)^{\frac{1}{2}}}{(p+q+1)(pq)^{\frac{1}{2}}} \quad \ldots\ldots(8)$$

Since, $\sigma_1 = \sqrt{\sigma_2}$

$$\sigma_1 = \sqrt{\frac{pq}{(p^2+q^2+2pq)\ (p+q+1)}} \quad \ldots\ldots(9)$$

Note that mean , variance , slew of the impulse response

$$\mu = -m_1 = \frac{p}{p+q} \quad \ldots\ldots(10)$$

$$\sigma_2 = 2m_2 - p_1^2 = \frac{pq}{(p+q)^2(p+q+1)} \quad \ldots\ldots(11)$$

$$\gamma_3 = -6m_3 + 6m_1m_2 - 2m_1^3 = \frac{2(q-p)(p+Q+1)^{\frac{1}{2}}}{(p+q+2)(pq)^{\frac{1}{2}}} \quad \ldots\ldots(12)$$

For, $p \succ 1, q \succ 1$

$$p = \frac{m\left[n - \left(n^2 - 4mp\right)^{\frac{1}{2}}\right]}{2m(1+m_1)} \quad \ldots\ldots(13)$$

$$q = \frac{-n + \left(n^2 - 4mp\right)^{\frac{1}{2}}}{2m} \quad \ldots\ldots(14)$$

Where r,s,t can be calculated by given formulae

$$r = 2m_1^4 - 6m_1^2m_2 + 6m_1m_2$$

$$s = 4m_1^5 + 4m_1^4 - 12m_1^3m_2 - 12m_1^2m_2 + 12m_1^2m_2 - 12m_1^2m_3 + 12m_1m_3 - 4m_1 - 2$$

$$t = -2m_1^2 - 3m_1 - 1$$

The mode is obtained as[12]

$$\mathrm{mod}\, e = \frac{p-1}{p+q-2}$$

Now the Expression for the Median i.e. 50% delay is given by [13]

$$median = \frac{1}{3}[\mathrm{mod}\, e + 2mean]$$

$$median = \frac{1}{3}\frac{3p^2+3pq-5p-q}{(p+q)(p+q+2)} \quad \ldots\ldots(15)$$

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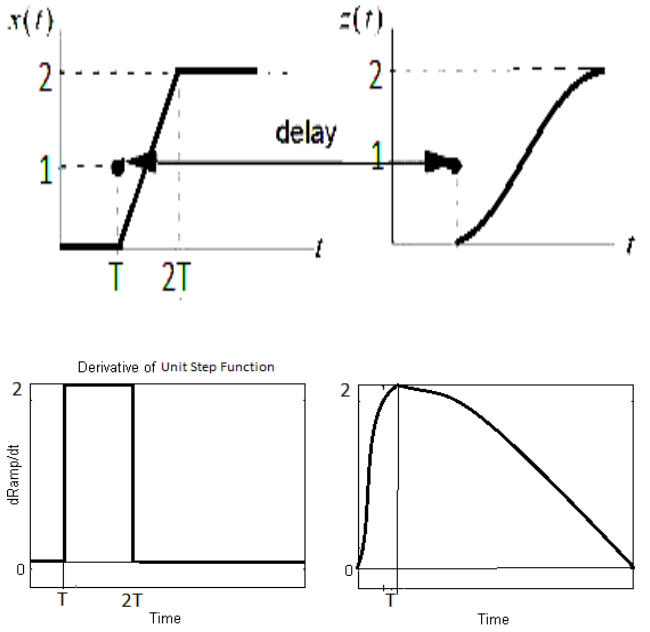
III.II Extension for the ramp input

In the figure we showed step function with delay and ramp function with delay and its probability distribution function of step and ramp. Now let us assume input of ramp with slope 2 on x- axis and delay of (T) on y axis and its PDF is also slope has 2. now we have draw step input With delay (T) and magnitude 2and draw its PDF.



Ramp and its PDF Output and its PDF

Fig.2.Ramp input and its corresponding response of an RLC circuit

IV Experimental Result

we can implemented proposed delay by using gamma distribution. Now we use RLC interconnected circuit when the driver is voltage source followed by resistor

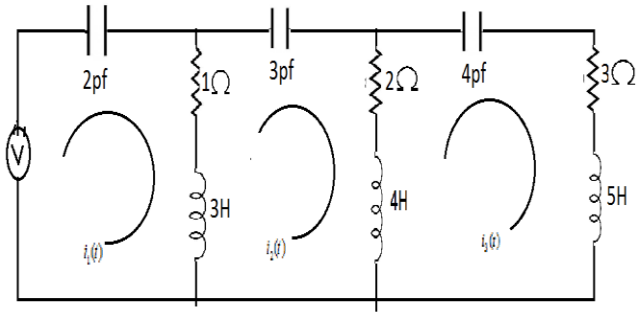


Fig.3. RLC example

Now apply KVL in mesh 1

$$V(t) = \frac{1}{2}\int i_1(t)dt + 1[i_1(t) - i_2(t)] + 3\frac{d}{dt}[i_1(t) - i_2(t)]$$

Now taking Laplace transform, we get

$$\frac{1}{s} = \frac{1}{2}\frac{i_1(s)}{s} + 1[i_1(s) - i_2(s)] + 3[si_1(s) - si_2(s)]$$

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$$\frac{1}{s} = i_1(s)\left[\frac{1+2s+6s^2}{2s}\right] - i_2(s)[3s+1] \quad \text{.....(16)}$$

Now apply KVL in mesh 2

$$0 = 1[i_2(t) - i_1(t)] + 3\frac{d}{dt}[i_2(t) - i_1(t)] + \frac{1}{3}\int i_2(t)dt + 2[i_2(t) - i_3(t)] + 4\frac{d}{dt}[i_2(t) - i_3(t)]$$

Now taking Laplace transform, we get

$$0 = [i_2(s) - i_1(s)] + 3[si_2(s) - si_1(s)] + \frac{1}{3}\frac{i_2(s)}{s} + 2[i_2(s) - i_3(s)] + 4[si_2(s) - si_3(s)]$$

$$0 = i_2(s)\left[\frac{21s^2+9s+1}{3s}\right] - i_1(s)[3s+1] - i_3(s)[4s+2] \quad \text{.....(17)}$$

Now apply KVL in mesh 3

$$0 = 2[i_3(t) - i_2(t)] + 4\frac{d}{dt}[i_3(t) - i_2(t)] + \frac{1}{4}\int i_4(t)dt + 3i_3(t) + 5\frac{di_4(t)}{dt}$$

Now taking Laplace transform

$$0 = 2[i_3(s) - i_2(s)] + 4[si_3(s) - si_2(s)] + \frac{1}{4}\frac{i_3(s)}{s} + 3i_3(s) + 5si_3(s)$$

$$0 = i_3(s)\left[\frac{36s^2+20s+1}{4s}\right] - i_2(s)[4s+2] \quad \text{.....(18)}$$

By solving above equations we get the values of current $i_1(s)$, $i_2(s)$ and $i_3(s)$

In order to verify the efficiency of our model, we have extracted 208 routed nets containing 1026 sinks from an industrial ASIC design in 0.18µm technology.

V CONCLUSION

In this paper we find accurate interconnect delay for VLSI design for step input and ramp input. Gamma distribution function is used to derive metrics and elmore delay model is upper bound signify less error and SPICE simulation result will obtained.

REFERENCES

[1] W.C.Elmore, "The transient response of damped Linear network with Particular regard to Wideband Amplifiers", J. Applied Physics, 19, 1948, pp.55-63.

[2] R.Kay and L.Pileggi, "PRIMO: Probability Interpretation of Moments for Delay Calculation",IEEWACM Design Automation Conference, 1998, pp. 463-468.

[3] Shien-Yang Wu, Boon-Khim Liew, K.L. Young, C.H.Yu, and S.C"Analysis of Interconnect Delay for 0.18µm Technology and Beyond" IEEE International Conference Interconnect Technology, May 1999 , pp. 68 - 70

[4] T. Lin, E. Acar, and L. Pileggi, "h-gamma: An RC Delay Metric Based on a Gamma Distribution Approximation to the Homogeneous Response", IEEE/ACM International Conference on Computer-Aided Design, 1998, pp. 19-25.

[5] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", Tran. on CAD, Volume 9, Issue 4, 1990. pp. 331- 349

[6] R. Gupta, B. Tutuianu, and L. T. Pileggi, "The Elmore Delay as a Bound for RC Trees with Generalized Input Signals", IEEE Trans. on CAD, 16(1), pp. 95-104, 1997.

[7] H. J. Larson, "Introduction to Probability Theory and Statistical Inference", 3rd ed., John Wiley & Sons pub., 1982.

[8] M. G. Kendall and A. Stuart, "The Advanced Theory of Statistics, vol. 1: Distribution Theory", New York: Hafner, 1969.

[9] H. L MacGillivray, "The Mean, Median, Mode Inequality and Skewness for a Class of Densities", Australian J. of Statistics, vol. 23 no. 2, 1981.

[10] C. Chu and M. Horowitz, Charge-Sharing Models for Switch Level Simulation, Trans. on CAD, Volume 6, Issue 6 June, 1987.

[11] Harald Cramer. Mathematical Methods of Statistics. Princeton University Press, 1946.

[12] M. Celik, L. Pileggi, A. Odabasioglu, "IC Interconnect Analysis" by Kluwer Academic Publishers, 2002.

[13] Chandramouli V. Kashyap, Charles J. Alpert, Frank Liu, and Anirudh Devgan, "PERI: A Technique for Extending Delay and Slew Metrics to Ramp Inputs" Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems 2002, pp. 57 – 62

[14] Chandramouli V. Kashyap, Charles J. Alpert, Frank Liu, and Anirudh Devgan, "Closed Form Expressions for Extending Step Delay and Slew Metrics to Ramp Inputs", International Symposium on Physical Design archive Proceedings of the 2003 ,Pages: 24 - 31

[15] Amandeep Kour, Vimal kishore Yadav, Vikas maheshwari, Deepak Prashar, "Face Recognition Using Template Matching", " IEEE International Conference on Signal and Image Processing (ICCSP), April. 3rd-5th, 2013, Melmaruvathur, Tamilnadu.

[16] Amandeep Kour, Vimal kishore Yadav, Vikas maheshwari, Deepak Prashar, "Web Mining in Soft Computing Relevance and Future Directions Delay", International Journal of Electronics Communication and Computer Engineering, vol. 4, Issue 1 ISN(online):2249-071X, ISSN(print):2278-4209, 2013.

[17] Amandeep Kour, Vimal kishore Yadav, Vikas maheshwari, Deepak Prashar, "A Review on Image Processing" International Journal of Electronics Communication and Computer Engineering, vol. 4, Issue 1 ISN(online):2249-071X, ISSN(print):2278- 4209, 2013.

[18] Vikas Maheshwari, Prabhakar Sharma, Alka Goyal, Vimal K Yadav, Sampath Kumar,"Closed Form Expressions for Delay to Ramp Inputs for On-Chip VLSI RC Interconnect",National Conference on Emerging Trends in Electrical, Instrumentation & Communication Engineering, vol. 4, Issue 7 ISSN 2222-1727, (Paper) ISSN 2222-2871 (Online), 2013.

[19] Vikas Maheshwari, Shruti Gupta, Kapil Khare,Vimal Yadav,Rajib Kar, Durbadal Mandal,Anup Kr. Bhattacharjee, "Efficient Coupled Noise Estimation For Rlc On-Chip Interconnect", Ieee Symposium On Humanities, Science And Engineering Research (Shuser-2012), Kuala Lumpur, Malaysia, Pp. 1125-1129,June 24-27, 2012.

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BIOGRAPHIES

VIMAL KISHORE YADAV Passed B.Tech degree in Electronics and engineering from Anand E ngineering college, Agra, U.P Technical University Lucknow. He served as an Assistant Professor in ECE department at Hindustan College of Science and Technology Mathura. He has published 2 Papers in International conference in IEEE and 4 papers in International Journal. He is perused his M.Tech in Energy Science and Engineering at IIT Bombay, Mumbai, India and Presently working as A. Professor at AMITY University, MP,INDIA

SUCHETA YADAV Passsed B.tech in Electronics and Communication Engineering from RJIT,Gwalior,MP. She had work experience of 4 year as Asst. Professor at Dr.K.N.M.I.E.T Modinagar.she Completed her M.tech from RGPV,MP

PRATIKSHA SINGH GAUR Passed B.Tech in Electronics and Communication Engineering from College Of Science And Engineering Jhansi, U.P Technical University Lucknow. I had done my final year project on Microstrip Antenna(Wireless Communication) and done my training on BSNL and All India Radio Prasar Bharti I pursuing M.Tech from Amity University Gwalior, Madhya Pradesh

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