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Survey on Performance of Vedic Multiplier

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Abstract: It is important to develop a high-performance multiplier architecture to meet the requirements of real-time, low power, low cost and small area in different applications. Vedic multiplier is one such promising solution and its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. In this paper various types of Vedic sutras are discussed and extensive survey on features of the Vedic multiplier design were reported.

Keywords: Vedic multiplier, Vedic mathematics, high speed and low power.

I.INTRODUCTION

Vedic mathematics was proposed by former Jagadguru Sankaracharya of Puri and he proposed a set of 16 sutras (aphorisms) and 13 sub-sutras (corollaries) from the Atharva Veda and then he developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries, founded by Swami Bharati Krishna Tirtha (1884-1960), and named it as Vedic mathematics. Hence there has been considerable literature on mathematics in the Veda-sakhas. Regrettably most of its has been bygone to humanity until now. It has been evident from the fact that meanwhile, by the time of patanjali, about 25 centuries earlier, 1131 Veda-sakhas were known to the Vedic scholars and only about ten Veda-sakhas are presently in the knowledge of the Vedic scholars in the country. The Vedic sutras can be applied to various problems and covers almost every branch of mathematics. They can be applied even to multiplex problems involving a large number of mathematical operations [2]. The application of sutras saves a lot of time and effort in solving the problems, when compared to the formal methods presently prevailing in this field. Despite the solutions appear mysterious, the application of the sutras is perfectly logical and rational. The computation made on the computer chase in a way, the principles implicit in the sutras. The Vedic sutras provide not only methods of calculation, but also give a way of thinking for their application.

II. VEDIC MATHEMATICS

The Sanskrit word 'Veda' is derived from the root word 'Vid', meaning to know without limit. The word 'Veda' covers all Veda-sakhas known to the humanity. The Veda is a repository of all knowledge, fathomless, ever revealing as it's delved intense.

It is mainly based on the 16 sutras which deal with various fields of mathematics such as algebra, geometry, calculus etc. Therefore the application of Vedic sutras to specific problems in Mathematics involves rational thinking, which helps the process improve intuition. It provides mental and super fast technique along with quicker cross-checking systems. The Vedic math's converts complex calculations into a playful and blissful one which students learn with smiles. It is based on pattern recognition and hence allows for constant expression of a student's creativity, and it is to learn. [7] The element of choice and the flexibility at each stage keeps the mind lively and alert to develop clarity of thought and intuition, hence a holistic development of the human brain automatically takes place during the process. It has an inbuilt potential to solve the problems of mathematics psychologically and also with anxiety [2].

III. VEDIC SUTRAS

In Vedic mathematics technique for any problem there is always one general technique applicable to all cases and also a number of special pattern problems. It is mainly based on 16 main sutras and 13 sub-sutras which can be given as follows:

A. Sutras

1. Ekhadhikena Purvena – By one more than the previous one.
2. Nikhilam Navatascaramam Dasatah – All from 9 and the last from 10.
3. Urdhva-Tiryaghbhyam – Vertically and crosswise.
4. Paravartya Yojayet – Transpose and adjust.
5. Shunyam Samayasamuccaye – when the sum is the same that sum is zero.
6. (Anurupye)Shunyamanyet – If one is ratio, the other is zero.
7. Sankalana Vyavakalanabhyam – By addition and by subtraction.
8. Puranapuranabhyam – By the completion or non-completion.
9. Chalana-Kalanabhyam – differences and similarities.
10. Yaavadunam – Whatever the extent of its deficiency.
11. Vyashtisamanstih –Part and whole.
12. Shesanyankena Charamena – The remainders by the last digit.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Ekanyunena Purvena – By one less than the previous one.
15. Gunitasamuchayah – The product of the sum is

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equal to the sum of product.
16. Gunakasamuchayah – The factors of the sum is equal to the sum of factors.

B. Sub-sutras
1. Anurupyena.
2. Shishyate Sheshamjnah.
3. Adyamadye Nantyamantyena.
4. Kevlaih Saptakam Gunyat.
5. Vestanam.
6. Yavadunam Tavadunam.
7. Yavadunam Tavadunikutya Vargankach Yojayet.
8. Antyayor daskepi.
9. Antyayoreva.
10. Samuchayagunitah.
11. Lopanasthapanabhyam.
12. Vilokanam.
13. Gunitasamuchayah samuchayahgunitah.

Vedic mathematics is one of the most delightful chapters of the 20th century mathematical history. It has great educational value because the sutras contain techniques for performing some elementary mathematical operations in simple ways and results are obtained quickly. Hence Vedic mathematics is facile to learn, faster to use and less liable to fallacy than conventional method [4].

IV. VEDIC MULTIPLIER DESIGN

A. Urdhva-Tiryaghbhyam sutra: Urdhva-Tiryaghbhyam sutra is known as "vertically and crosswise" and it is a general multiplication formula which can be applied to all type of multiplication. The specialty of this sutra is that partial product generation and addition can be done simultaneously at the same time. It is more efficient in binary multiplication and it is suitable for parallel processing which in turn reduces delay in a design [5]. The multiplication scheme can be explained by the following example as shown below in figure 1.

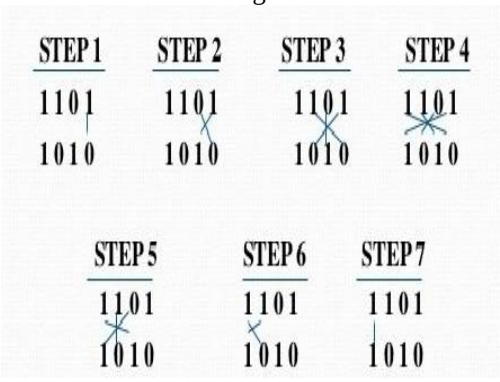

Fig. 1 Example of Urdhva-Tiryaghbhyam using binary multiplication

This sutra is generally used for the multiplication of binary numbers and the multiplication formula can be applicable to all types of multiplication. In Vedic multiplier the computation time is less when compared with other multipliers and it is independent of clock frequency. Due to its regular structure it can be realized easily in a silicon chip [6].

B.Nikhilam navatascaramam dastah: Nikhilam sutra is simply known as "All from 9 and the last from 10". The sutra can be very efficaciously applied in multiplication of numbers, which are nearer to basis like 10, 100, 1000 hence, to the power of 10[1]. The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and need only intellectual calculation. The numbers taken can be either less or more than that of the base considered. The dissimilarity between the number and the base is known as deviation. Deviation may be either positive or negative. The positive deviation is written without the positive sign and the negative deviation, is written using rekhank (a bar on the number). An example for nikhilam sutra is shown below in figure 2.

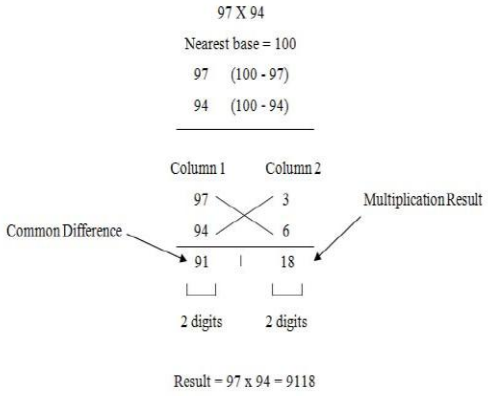

Fig. 2 Example for Nikhilam sutra

The deviations obtained by the nikhilam sutra can be called as Nikhilam multiplication method [7].

C. Paravartya Yojayet: Paravartya Yojayet means "Transpose and adjust" and its corollary is kevalaih saptakam gunyat. This method is related to the Chinese remainder theorem and the Horner's rule of the synthetic division, but possibly has even more applications which are given below in figure 3.

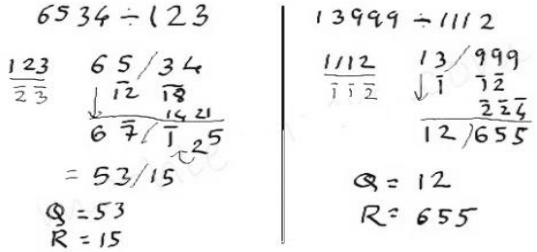

Fig. 3 Example for Paravartya Yojayet

This sutra contains a brief and incomplete summary of the math shortcuts in which the divisor is more than one digit and slightly higher than a power of 10. It can also used for numbers slightly higher than 100, 1000 and etc[1].

D. Gunakasamuchayah: The sutra says 'All the multipliers' means the product of the sum of the coefficients in the factors is equal to the sum of the

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coefficients in the product. This sutra is useful in verifying the correctness of the obtained answers in multiplication, division, and factorization [3]. This rule holds true all the cases cubic's and biquadrate's, etc.

i.e., Sc of the product = Product of the Sc

V. SURVEYED DESIGNS

S.Kokila et.al. (2012) analyzed VHDL implementation of fast 32×32 multiplier based on Vedic mathematics. High speed, low power, less area and delay can be achieved by designing multiplier in VHDL, as it give effective utilization of structural modeling. Usage of carry save addition in the multiplier architecture reduces the delay in the multiplier design. It provides a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics as shown in figure 4. The architecture of the designed Vedic multiplier comes out to be very similar to that of the popular array multiplier and hence it should be noted that Vedic mathematics provides much simpler derivation of array multiplier than the conventional mathematics.

Many digital signals processing operation requires several multiplication and for the same we need very fast multiplier for a wide range of requirements for hardware and also for high speed applications. This paper presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics.

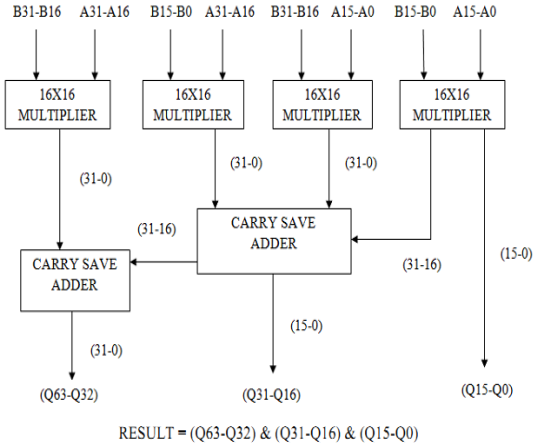

Fig. 4 32×32 bit Vedic multiplier Block Diagram

It consumes less power when compared with other multiplier designs and the design complexity gets reduced for inputs of large number of bits and modularity gets increased.

Padmanabin Gopalakrishna and Gangavarapu Kiran Kumar (2013) described modeling of towering speed and area competent Vedic multiplier using Urdhva-Tiryaghbhyam sutra. The implemented design is efficient in terms of area and speed compared to its implementation using array and booth multiplier architecture. It can be easily implemented in hardware and by using basic nibble multiplication unit, the higher bit multiplication can be construct which will make modification easier as shown in figure 5.

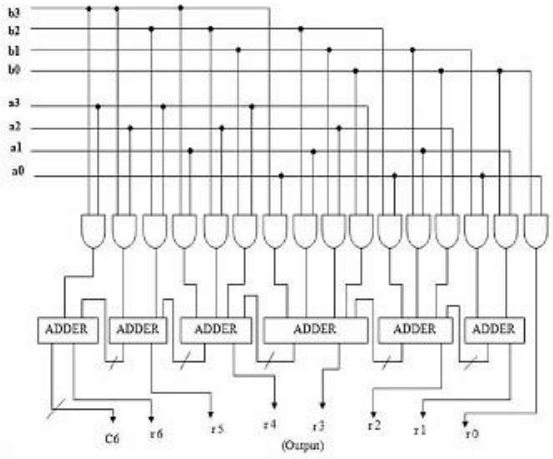

Fig. 5 Hardware Architecture of the Vedic multiplier[8]

The implemented design made debugging easier and efficient in area and speed and hence area consumption is less. Therefore the multiplier architecture uses fewer resources such as less number of multipliers and adders and is flexible in design.

Kavita and Umesh Goyal (2013) described FPGA implementation of Vedic multiplier which is implemented by using Gunakasamuchayah sutra. The implemented design is more efficient and fast as compared with other multipliers and the number of look up tables required to implement the multiplier is also less when compared with other multipliers.

Leonard Gibson Moses S and Thilagar M (2010) designed a high speed DSP algorithms using Vedic mathematics which is implemented in VLSI. The design of various N×N multipliers has been analyzed thoroughly by using the techniques like Urdhva-Tiryaghbhyam, Nikhilam and Anurupye for arithmetic multiplications. The UT is more efficient sutra in this design and it gives minimum delay for multiplication of all types of numbers. Using this method single precision floating point multiplication has been designed as shown in figure 6.

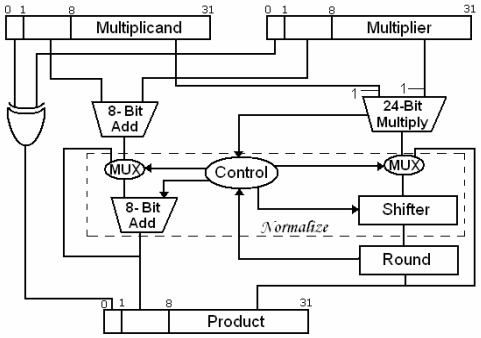

Fig. 6 Single Precision Floating Point Multiplication Architecture[5]

Hence the Vedic Multiplication method decreases the area and speed up the combination by using small number of logic elements and short-cut methods.

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R.P.Meenaakshi sundari et.al. (2013) analyzed enhancing multiplier speed in fast fourier transform based on Vedic mathematics and designed a high speed multiplier using Urdhva-Tiryaghbhyam, Nikhilam and Anurupye sutras.

The algorithm gives minimum delay and used for multiplication of all types of numbers and the performance of the multiplier is compared using these sutras for various N×N multiplications and implemented on the FFT of the DSP processor.

The Anurupye sutra is more efficient than UT and Nikhilam by more reduction in the computation time and delay is considerably reduced in this design.

Diganta Sengupta et.al. (2013) analyzed Vedivision - A Fast BCD division algorithm facilitated by Vedic mathematics to achieve a generalized algorithm for BCD division which is efficient and optimized than the conventional algorithms in literature as shown in figure 7.

The Nikhilam sutra provides better results when division requires large divisors. If the divisor is a small number, the sutra provides an ambiguous result which was rectified by another sutra known as Paravartya Yojayet.

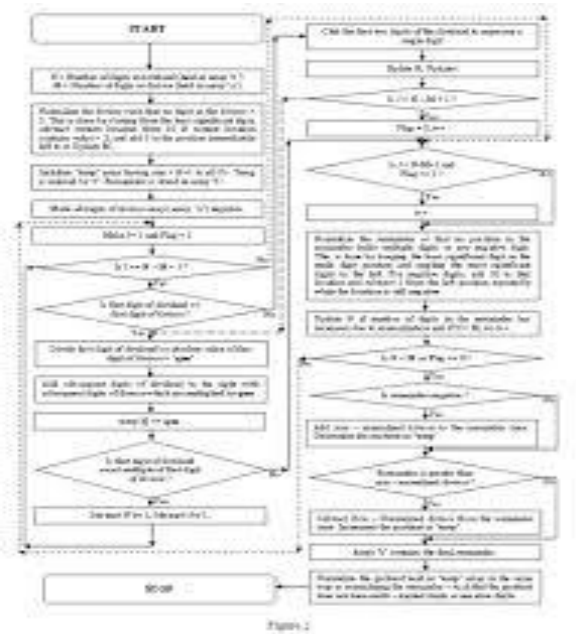

Fig. 7 Flow chart of Vedic Division Algorithm [1]

The execution time of the design does not depend on the size of the dividend or the divisor, instead of that it is based on the number of remainder normalizations required in the design.

VI. CONCLUSION

In this paper various types of Vedic multiplier is designed based on the Vedic sutras to achieve low power consumption, less area, high speed, fast and reduced computation time. Vedic multipliers can be implemented in different fields of applications. This paper made a brief analysis of Vedic multipliers using different types of Vedic sutras.

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BIOGRAPHIES

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