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FPGA implementation of cordic algorithm used in DDS based modulators

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Abstract: The modern communication systems and software radio based applications demands smart transceivers, consisting of only an antenna and a fully programmable circuit with digital modulators and demodulators. A basic communication system's transmitter modulates the amplitude, phase or frequency proportional to the signal being transmitted. An efficient solution (that doesn't require large tables/memory) for realizing universal modulator is CORDIC (CO-ordinate Rotation Digital Computer) algorithm. The CORDIC algorithm is used in the rotation mode, to convert the coordinates from polar mode to rectangular mode. CORDIC is a versatile algorithm widely used for VLSI implementation of digital signal processing applications. This paper presents how to use CORDIC to implement different communication subsystems that can be found in software defined radio. Specifically, it shows how to use CORDIC to implement direct digital synthesizers and ASK, PSK, FSK Modulators. The focus of this paper is to analysis and simulation of ASK, FSK, PSK modulation scheme using Direct Digital Synthesizer having CORDIC algorithm at the place of ROM Look up Table. CORDIC Algorithm provides many significant advantages over Conventional ROM Look up Table.

Keywords: Software Defined Radio, CORDIC algorithm, DDS, ASK, FSK, PSK.

I INTRODUCTION

The Coordinate Rotation Digital Computer (CORDIC) was introduced in 1959 by Volder [1]. It is an easy-to-implement and versatile algorithm widely used for digital signal processing applications. It computes iteratively the rotation of a two-dimensional vector using only add and shift operations. CORDIC has been traditionally used for hardware implementations. In [2] several algorithms which admit efficient implementation using CORDIC were reviewed: linear transforms, digital filtering, and matrix based DSP computing algorithms. It was shown that CORDIC-based architectures are a very appealing alternative to conventional multiply-and-add hardware. However, CORDIC may be also applied to implement different communication subsystems found in a digital radio: direct digital synthesizers; amplitude shift keying (ASK), phase shift keying (PSK), and frequency shift keying (FSK) modulators.

II CORDIC FUNDAMENTALS

For an easy understanding of how to use the CORDIC algorithm in the implementation of digital intermediate frequency (IF) communications systems, CORDIC is presented only as a computational resource with three inputs (X_0, Y_0, and Z_0) and three outputs (X_N, Y_N, and Z_N) that allows performing the following operations[3]as shown in Figure 1.

• Rotation Mode (RM): Rotation of a vector (I, Q) by an angle q when it is operating in rotation mode (RM); the rotated output vector is multiplied by a constant value K.

•Vectoring Mode (VM): Cartesian-to-polar conversion, when it is operating in vectoring mode (VM); the modulus of the vector is also scaled by K.

A generic scheme that shows how to use RM CORDIC to implement different digital communication tasks is shown in Figure1. The scheme is composed of an RM CORDIC where signals I and Q are connected into X_0 and Y_0inputs, and the phase term q connected into Z_0 input is $q = (\sum[fc + fm]) + \emptyset m) \times \pi$.

This phase term is composed of the accumulation, at a sample period of Ts, of two frequency terms, f_c and f_m, and a phase term, $\emptyset_m$ The additions involved in its computation are signed modulo-1 (limited to the interval [–1,1]), and the frequency and phase terms f_c, f_m and $\emptyset_m$ are normalized to 1. The CORDIC Z_0 input needs a phase input that takes values in the interval [–π, π], so a multiplication by π is required to extend the interval of the normalized term q to the interval required by CORDIC [3].

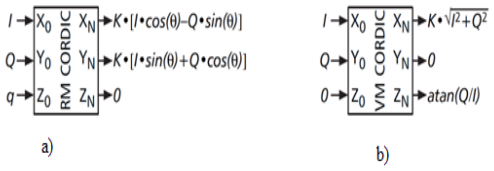

Figure 1 a) Rotation mode b) vectoring mode CORDIC.

CORDIC computes a pseudo-rotation of a two-dimensional vector instead of perfect rotation. This means that the original vector is rotated by an angle q, and its magnitude is enlarged by a constant factor K.

The CORDIC algorithm iteratively computes the pseudo-rotation by an angle q with the following iterations:

$$X_{i+1} = [X_i - d_i \times 2^{-i} \times Y_i]$$
$$Y_{i+1} = [Y_i + d_i \times 2^{-i} \times X_i] \quad (1)$$
$$Z_{i+1} = Z_i - d_i \times a_i$$

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Instead of directly performing a rotation by the angle q, CORDIC performs several micro-rotations by the angles $a_i = \pm atan\ (2^{-i})$. This means that the rotation angle q is broken down into a set of predefined angles a_i, so after a number of iterations the angle q is approximated by $\sum (d_i \times a_i)$, where *di* belongs to the set {–1, 1}. CORDIC Eq. (1) admits two operating modes, the rotation mode (RM) and the vectoring mode (VM), which depend on how the directions of the micro rotations (d_i) are chosen: $d_i = sign\ (Z_i)$ for RM and $d_i = -sign\ (Y_i)$ for VM.

III CORDIC ALGORITHM BASED COMMUNICATION SYSTEM

A. DIRECT DIGITAL SYNTHESIS

Direct digital synthesis is a method to generate waveforms directly in the digital domain. In communications systems the target waveforms are the sine and cosine ones. A DDS is composed of a phase accumulator and a phase-to amplitude converter [3], as shown in Fig. 2 a. In a conventional DDS based on lookup tables (LUTs) the phase accumulator is an integer *N*-bit accumulator (an unsigned modulo-2^N accumulator), whose output directly addresses the LUT where the amplitude values of sine or cosine waves are stored. The maximum value of the accumulator (2^N–1) represents the phase 2 π of the sine or cosine wave. The accumulator generates a ramp signal when it is incremented by a fixed value, due to its unsigned modulo-2^N property; hence, a periodic waveform is obtained at the output of the phase-to-amplitude converter (Fig. 2 b).

The CORDIC algorithm configured in RM can behave as a quadrature phase-to-amplitude converter that directly generates sine and cosine waveforms [4]. The main advantage of using CORDIC-based DDS with respect to LUT based methods is that it can achieve both high phase resolution and high precision with lower hardware cost [5]. A difference between both methods is that the phase accumulator generates an integer value that addresses an LUT in the LUT-based method, while it generates an angle in CORDIC-based DDS. Thus, in the last case a ramp signal in the interval [–π, π] must be obtained by the accumulator, as shown in Fig. 2c. This accumulator is easily implemented with an *N*-bit adder. A two's complement fractional numeric format (only one integer bit) is considered; hence, a ramp in the interval [–1, 1] is generated, and a multiplier by π is introduced to achieve the desired range.

To generate sine and cosine waveforms of a digital frequency f_c with the scheme based on CORDIC of Fig. 3, the parameters f_m, ϕ_m, and *Q* must be zero and I = 1/*K*. The oscillation frequency is controlled by giving a fixed value to *fc*. In such a case CORDIC generates directly the cosine and sine waveforms ($s_i(n) = cos(f_c.\ \pi\ n)$ and $s_q(n) = sin(f_c\ .\ \pi\ .n)$) through X_N and Y_N outputs, respectively. The maximum synthesized frequency is obtained by taking the value f_c = 1 (which is equivalent to analog frequency of $f_s/2$); and the minimum frequency is achieved with $f_c = 2^{-(N-1)}$, where *N* is the word-length of the accumulator [6-7].

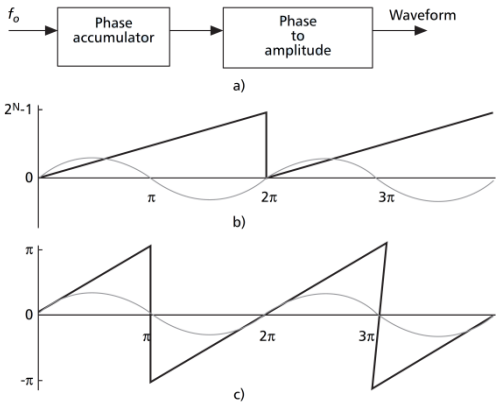

Figure 2 a) DDS block diagram; b) waveforms of the LUT-based method; c) waveforms of the CORDIC-based method

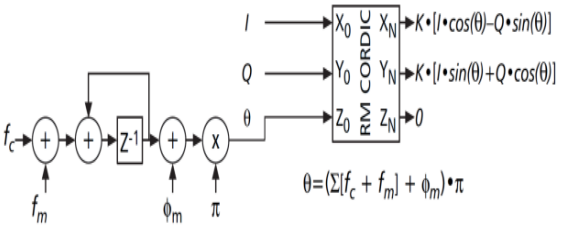

Figure 3 Generic scheme to use CORDIC in Rotation Mode.

B. FREQUENCY, PHASE AND AMPLITUDE MODULATORS

The CORDIC scheme of Fig. 3 can be used to directly generate in the digital domain at IF the binary modulations ASK, PSK, and FSK.

The CORDIC scheme of Fig. 3 can be used to directly generate in the digital domain at IF the binary modulations ASK, PSK, and FSK [8]. Considering *m*(*n*) as the modulator signal, ASK can be implemented by choosing in Fig. 3 carrier IF f_c, using the input *Xo* as modulator signal $I = m(n)/K$, and leaving to zero f_m, $\emptyset_m$, and *Q*. In such a case the ASK signal ($s(n) = m(n) \times cos(f_c \times \pi \times n)$) is generated through X_N CORDIC output. If PM is desired, the terms f_m and *Q* of Fig. 3 are zeroed, the input X_o is fixed to $I = 1/K$, and the phase modulator signal is $\emptyset_m = m(n)$. Then the PM signal ($s(n) = cos(f_c \times \pi \times n + m(n) \times \pi$)) is obtained with a carrier frequency f_c, through the X_N output. An FSK signal can be generated with the scheme of Fig. 3 if the frequency modulator signals is $f_m = m(n)$, the carrier frequency is a fixed value f_c, the terms $\emptyset_m$, and *Q* are zero and the X_0 input is $I = 1/K$. The FSK signal ($s(n) = cos(f_c \times \pi \times n + (\sum m(n)) \times \pi)$) is also obtained by the output X_N. In an ASK, PSK, or FSK modulator, it is required to up-sample the base-band modulator signal *m*(*n*) up to the sampling rate (f_s) of the CORDIC processor and DAC. As this signal usually is a narrow band one, a Cascade-Integrator- Comb filter (CIC) is a very low hardware cost solution to perform this task [9].

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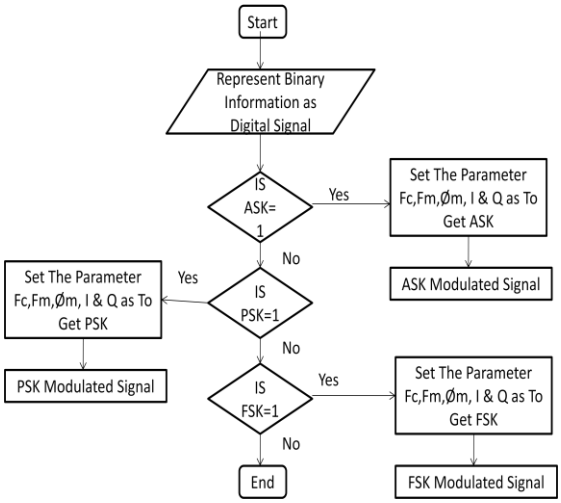
The flowchart used to do the programming in matlab and VHDL is as follows.



IV RESULTS AND DISCUSION

A. MATLAB SIMULATION

To visualize the result into waveform we need the matlab simulation. Here are the results of multimode system. The modulating signal is

$m(n)$=1001010101

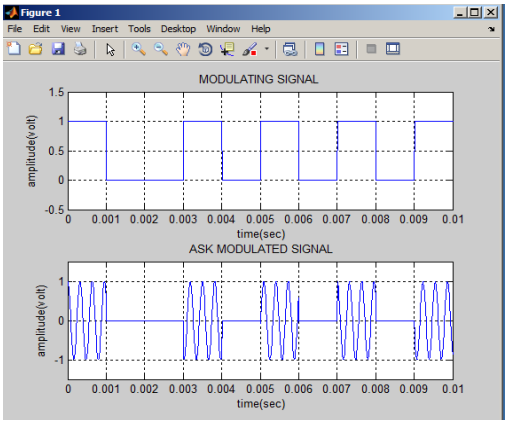


Figure 4 ASK modulated output in matlab simulation

When we select the mode ask =1we get the ASK output as shown in above figure 4.

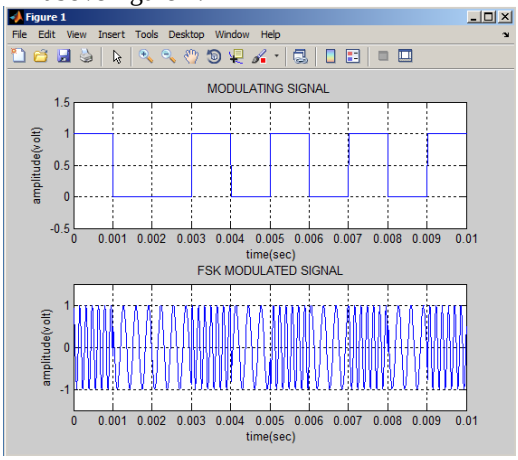


Figure 5 FSK modulated output in matlab simulation

When we select the mode fsk =1we get the FSK output as shown in above figure 5.

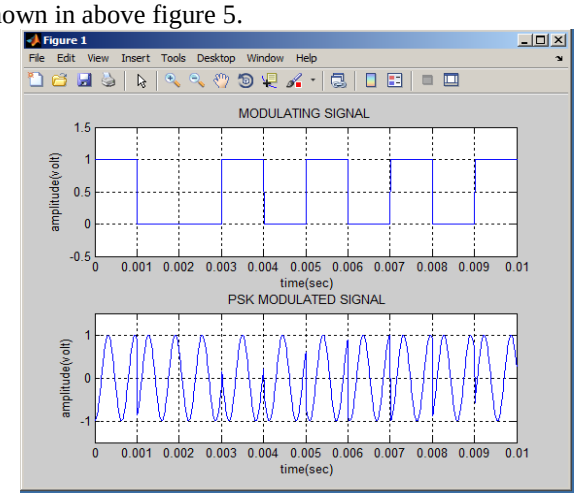


Figure 6 PSK modulated output in matlab simulation

When we select the mode psk =1we get the PSK output as shown in above figure 6.

B. VHDL SIMULATION OF DIRECT DIGITAL SYNTHESIS

The code was synthesized using XILINX ISE 13.1 and implemented on Spartan 3E FPGA board [10]. The simulation results are shown below:

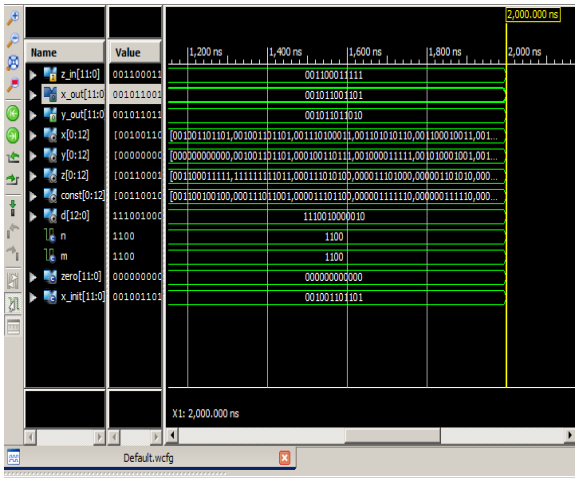


Figure 7 DDS output in VHDL simulation

The input given in this case is angle 0.781 and the respective Sine and Cosine function values are generated and as clearly shown in the figure 7 . T he values of both functions change per iteration and after the 1 2 iterations the final values are obtained.

The angle input is given in radians in binary format as given below

Z_in: “001100011111” =>00.1100011111 => 0.781

The DDS output we get as shown in figure 7 is

Xout: “001011010111” => 00.1011001101=> 0.710≈ cos(0.781)

Yout: “0010110100” => 00.1011011010 => 0.703≈ sin (0.781)

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C. VHDL SIMULATION OF DIGITAL MODULATION SCHEMES

The Digital modulation schemes such as of binary amplitude-shift keying (ASK), binary frequency shift keying (FSK) and binary phase-shift keying (PSK) was designed separately using Xilinx ISE 13.2 tool and its simulated results are shown below.

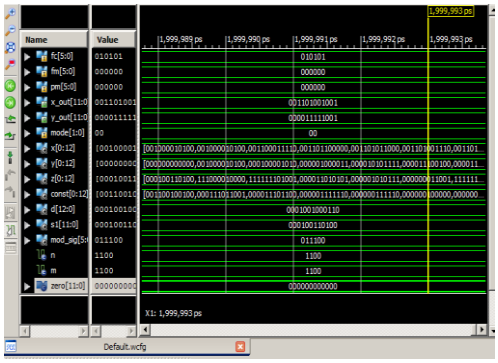

Figure 8 ASK modulated output in VHDL simulation

For ASK the input and outputs are given bellow and are clearly shown in figure 8.
Fc=carrier frequency=010101
Mod_sig=Modulating signal=011100
Mode=00
ASK signal= X_out= 001101001001.

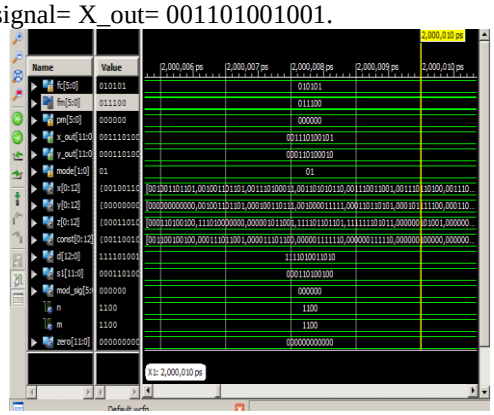

Figure 9 FSK modulated output in VHDL simulation

For FSK the input and outputs are given bellow and are clearly shown in figure 9.
Fc= carrier frequency =010101
Fm= Modulating signal =011100
Mode=01
FSK signal =X_out= 001110100101.

Figure 10 PSK modulated output in VHDL simulation

For PSK the input and outputs are given bellow and are clearly shown in figure 10.
Fc= carrier frequency =010101
Pm= Modulating signal =011100
Mode=10
PSK signal =X_out= 001111110101.
The design is interfaced with onboard LED display. The code was then successfully implemented on Spartan3E board after successful completion of translate, map, place and route processes. And the outputs can be viewed on LED display. The outputs for the above taken example for angle 0.781 are shown displayed on FPGA. The display shows the final value of Cos (0.781) to validate the implementation.

V CONCLUSION

This paper proposes the use of CORDIC algorithm for Direct Digital Synthesizer. CORDIC algorithm is an interesting technique for phase to sine amplitude conversion. The algorithm proposed in this design is to utilize dynamic transformation rather than ROM static addressing. The proposed CORDIC design is based on Pipeline data path Architecture. By using pipeline architecture, the design is able to calculate continuous input, has high throughput, and doesn't need ROM or registers to save constant angle iteration of CORDIC. CORDIC algorithm provides fast and area efficient computations of sine and cosine functions without using ROM LUTs. This paper is focused on the Direct Digital Synthesizer using CORDIC approach, to increase the speed with minimum area requirement in FPGA. Also this paper reveals that how to use the CORDIC algorithm to implement different blocks found in communications systems like ASK, PSK, and FSK digital modulators.

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