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AREA EFFICIENT DESIGN OF FIR FILTER USING SYMMETRIC STRUCTURE

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ABSTRACT: In this paper an area efficient method is presented to design and implement FIR filter. The proposed FIR filter has been implemented equiripple window using Transposed & Symmetric structure. The performance of two designs has been compared in terms of hardware requirements. The performance of both the designs is almost same but Symmetric structure has shown reduced hardware requirement as compared to Transposed structure. The proposed designs have been designed and simulated using Matlab 7.0.The Symmetric FIR filter has shown 55% reduction in multipliers as compared to Transposed structure for FIR filters. The Direct form transposed FIR filter produces the same output as the Direct form FIR but the cost varies in terms hardware requirements of Direct form Symmetric FIR. The difference is that it performs all the multiplications of a variable at the same time. The design time is also a key factor for low price products which is shown in implementation cost. The proposed FIR filter architecture is capable of operating for 16 bits word length filter coefficient. We show that dynamically reconfigurable filters can be efficiently implemented by using Direct form Symmetric FIR structure for equiripple FIR filter. Hence, an efficient design process aiming at high speed and great interest for minimizing total costs.

Keywords: DSP, FIR, MAC, FPGA.

I. INTRODUCTION

The demands for digital products with programmability are growing day by day. various industries like audio, video, and cellular industry rely heavily on digital technology. a great part of digital technology deals with digital signal processing. this aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology. Most of the common functions performed by almost all DSP chips are FFTs , FIR filters , Interpolator, Decimator. Finite impulse response (FIR) digital filters are common DSP functions and are widely used in FPGA implementations. If very high sampling rates are required, full-parallel hardware must be used where every clock edge feeds a new input sample and produces a new output sample.

In case fully parallel implementation is not possible then partly serial approach can be adopted to enhance the system performance. Such filters can be implemented on FPGAs using combinations of the general purpose logic fabric, on-board RAM and embedded arithmetic hardware. Full-parallel filters cannot share hardware over multiple clock cycles and so tend to occupy large amounts of resource. Hence, efficient implementation of such filters is important to minimize hardware requirement. When implementing a DSP system on a platform containing dedicated arithmetic blocks, it is normal practice to utilize such blocks as far as possible in reference to any general purpose logic fabric.

FPGAs are essentially arrays of uncommitted logic and signal processing resources [1]. These allow the designer to implement DSP functions using highly scalable, parallel processing techniques. There is a constant requirement for efficient use of FPGA resources where for a given system occupying less hardware can yield significant cost-related benefits like reduced power consumption, area for additional application functionality, potential to use a smaller, cheaper FPGA [2].

Reconfigurability and low complexity are the two key requirements of finite impulse response (FIR) filters employed in multi standard wireless communication systems. The fundamental idea of an SDR is to replace most of the analog signals in the transceivers with DSP in order to provide the advantage of flexibility by reconfiguration. This will enable different air-interfaces to be implemented on a

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single generic hardware platform to support multi standard DSP in wireless communications [3, 4]. The area of FIR filters increases with increase in filter order and higher filter order makes the hardware implantation difficult. A traditional DSP chip would perform the MAC FIR Filter function in serial manner where as an FPGA allows designers to implement this function in parallel style using dedicated multipliers and registers that are now available in recent FPGA [5]-[8].

Therefore, in this paper, an FIR filter is designed whose impulse response may be expressed as:

$$Y = \sum_{k=1}^{K} C_k x_k \qquad (1)$$

where C1,C2…….CK are fixed coefficients and the x1, x2…… xK are the input data words. A typical digital implementation will require *K* multiply-and-accumulate (MAC) operations, which are expensive to compute in hardware due to logic complexity, area usage, and throughput.

II. FIR FILTER

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. The output y of a linear time invariant system is determined by convolving its input signal x with its impulse response .For a discrete-time FIR filter, the output is a weighted sum of the current and a finite number of previous values of the input. The operation is described by the following equation, which defines the output sequence y[n] in terms of its input sequence x[n]. Processing of data quick enough to achieve real-time performance is a highly power-consuming task. Data is transferred through a network and filtered through filters containing multiplications and/or additions. The power consumed in such a filter is directly related to how many times multiplications or additions must be done. In this thesis the focus is on one-dimensional Finite Impulse Response (FIR) filters. The FIR-filter's equation is given in equation (1).

A direct form FIR filter design is shown in figure 1. A set of inputs are shifted through n number of registers (SR), also called "taps". They are then multiplied by a number of constant coefficients and added up. Basically a FIR filter is a data stream multiplied by a set of constants. The transposed form FIR filter is shown in figure 2.

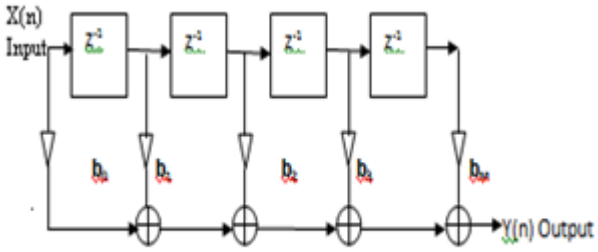

Figure1.The general FIR filter for Direct form -I

The transposed form of the FIR filter produces the same output as the direct form. The difference is that it performs all the multiplications of a variable at the same time. The shift registers are moved to delay the output from a multiplication instead of the input. This way different algorithm can be applied to the FIR filter. The main advantage of using FIR filters is that an exact linear-phase response can be obtained.

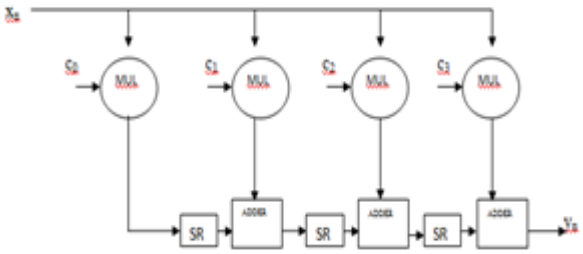

Figure2. Transposed FIR filter

To obtain this property, the impulse response must be symmetric or anti-symmetric around. This constraint may increase the filter order, however the symmetry can be exploited to reduce the hardware as shown in Figure 3.

Block finite impulse response (FIR) digital filters have potential for high-speed and low-power realization through parallel processing. In this paper, we suggest an efficient implementation of block FIR filters using multiple constant multiplication (MCM) technique. Constant multiplication methods are widely used for reducing computational complexity of implementation of FIR filters. Sub-expression sharing for single constant multiplications can be performed for direct-form as well as transposed direct-form structures of FIR filters, while MCM techniques are not applicable to

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the direct-form FIR structure. On the other hand block FIR filters cannot be implemented in transposed direct-form.

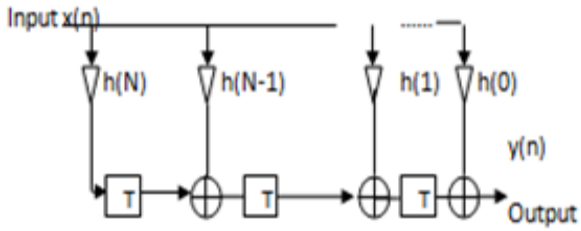


Figure3. Transposed Direct form filter structure

The multiplication with a constant can be replaced by a series of shifts and adders. The coefficients are depict in a transposed form FIR filtering shown in figure 3. The multiplication by coefficient a is shown as a series of adders and shifts in figure 3, and the multiplication by coefficient b is shown in figure 3.

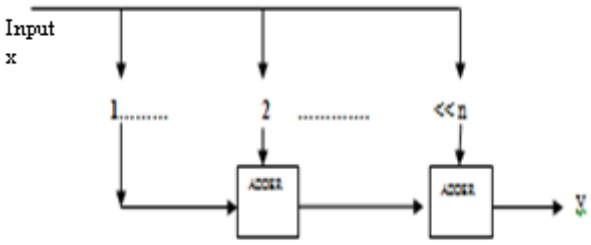
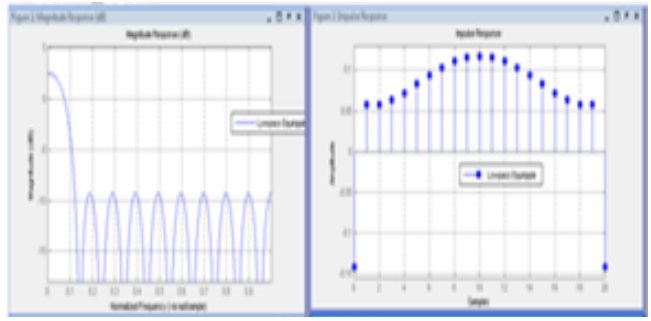


Figure 4.Multipication by coefficient a=1110 using additions and shifters

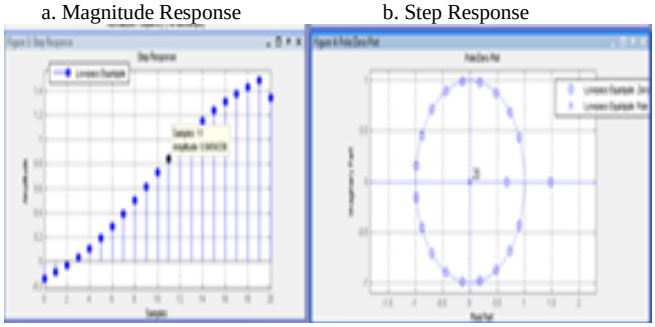
When comparing coefficient a and b it can easily be observed that two bits are in common for them, that being the 1st and the 3rd bit most significant bit. When constructing a filter where both coefficients are represented, their common digits can be exploited to reduce the number of adders needed shown in figure 4.

III. PROPOSED DESIGN SIMULATION

The 20 tap FIR filter has been developed and compared with the Transposed direct form and Symmetric structure. Equiripple based Symmetric FIR filter with compared with Transposed Direct form structure which is analysed and designed using Matlab7.0 [9]. The main advantage of Direct form Symmetric FIR is that it is no longer costly and can be operate on lower data sample rates.

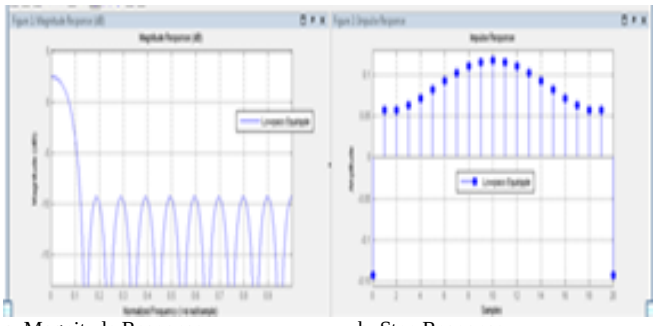


a. Magnitude Response b. Step Response

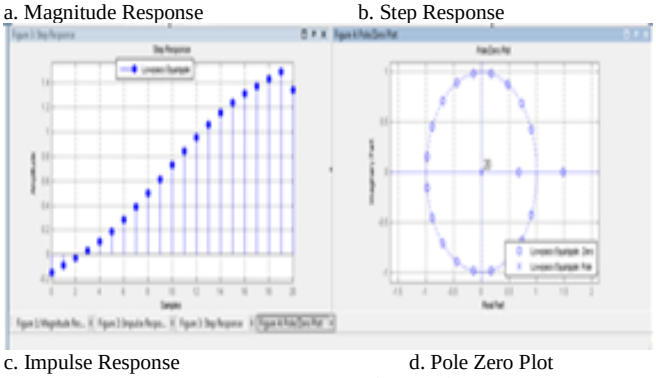


c. Impulse Response d. Pole Zero Plot

Figure 5. Various output response of Direct form Symmetric FIR



a. Magnitude Response b. Step Response



c. Impulse Response d. Pole Zero Plot

Figure 6. Various output response of Direct form Transposed FIR

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IV. HARDWARE REQUIREMENTS

The hardware requirements of both the designs have been calculated in terms of multipliers and adders to calculate the implementation cost. The emphasis is laid on the effect of the Transposed Direct Form structures and Symmetrical Direct form FIR filter. The implementation cost of two filters have been analysed and compared. The performances of both designs are almost identical but their implementation cost varies greatly, as shown in Table 1. The proposed Direct form Symmetric FIR filter results in efficient hardware saving in terms of multipliers and input sample per multiplier as compare to Transposed Direct form FIR filter.

TABLE I. Implementation Cost

DESIGN	Mult	Add	MPIS	APIS
Direct –Form FIR Transposed	21	20	21	20
Direct –Form Symmetric FIR	11	21	11	21

V. CONCLUSION

The cost effective design & 20 Tap FIR filter has been presented. The proposed design has been implanted using transformed direct form and Symmetric direct form structures. The design and simulation & proposed structure has been done using Matlab and implementation cost has been calculated in terms & multiplies and adders. The Symmetric structure has shown reduced consumed & multipliers. The Symmetric direct for FIR filter has consumed 21 multiplies as compared to 11 in case & transferred direct form FIR filter for providing cost and area efficiency. The transposed form of the FIR filter produces the same output as the direct form. The shift registers are moved to delay the output from a multiplication instead of the input. The proposed Direct form Symmetric FIR filter results in 55% hardware saving in terms of multipliers as compare to Transposed Direct form FIR filter.

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BIOGRAPHY

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