Analysed Modulation Doped Fieled Effect Transister (MODFET) and Metal Oxide Semiconductor Modulation Doped Fieled Effect Transister ((MOS-MODFET)) using compound material silicon Germanium (SiGe)

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Abstract: In this paper SiGe material incorporated to design Modulation Doped Fieled Effect Transister (MODFET) and analysed theoretically. The SiGe is a compound semiconductor material and impurity material is P-type. The Gate length of MOS-MODFET is fabricated 0.1μm. The SiGe/Si Heterojunction grown by ultrahigh vacuum chemical vapor deposition technique. The performance of modulation-doped field effect transistor is a new approached to design FET with heterojunction field effect transistor (HBT). The performance of MOS-MODFET is also a good approached to design device as CMOS with the HBT. The characteristics shown is improved the speed and power consumption with BJT and MOSFET.

Keywords: Modulation doping, MODFET, MOS-MODFET, and Characteristics

I. INTRODUCTION

CMOS digital circuits represent low-power consumption and the possibility of dynamic memories. Silicon Bipolar Junction Transistors (BJTs) are used about 20% of all integrated circuits, mostly high-speed and analog applications. The trend of increasing switching speeds and communication rates demands further improvement of the performance of BJT. In addition, at the present considerable number of BiCMOS circuits, which combine the high-current drive capability of BJTs with the low-power CMOS demonstrate new application for bipolar transistors [1]. The SiGe Heterojunction Bipolar Transistor (HBT) is one device that can meet these demands. Doped with III-V element in SiGe devices offer superior performance over silicon made device due to better material parameters as mobility and carrier velocity. The band-gap of SiGe is in beneath Si and Ge and the application of quantum effects have yielded new devices as, the modulation doped field effect transistor (MODFET). It has low noise.

II. MODULATION DOPING Si₁ₓGeₓ STRAINED LAYER

Heteroepitaxy of Si/Ge, Si₁ₓ,Geₓ offers exciting possibilities for integrated field-effect transistor (FET) structures [2]. In addition to such application, system also offers a unique opportunity to determine the effects of misfit strain on the transport properties of indirect gap semiconductor heterointerfaces and strained layer superlattices since the lattice mismatch between Si and Ge is ~4%. Recent progress in silicon molecular beam epitaxy (Si MBE) coupled with a quantitative determine of growth parameters pertinent to the pseudomorphic growth of GeₓSi₁₋ₓ/Si strained layers has made it possible to achieve the first two-dimensional hole gas at a Si/Ge₀.₂Si₀.₈ heterointerface.

III. MODFET STRUCTURE

The SiGe/Si heterostructure layer is grown by ultra high vacuum chemical deposition (UHV-CVD) on an n Si substrate. The layer sequence started with linearly step-graded Si₁₋ₓ,Geₓ buffer layer relaxed to the lattice constant of Si₀.₇Ge₀.₃. A 1μm-thick Si₀.₇Ge₀.₃ buffer layer is followed by the modulation-doped structure which consisted a 4-nm B-doped Si₀.₇Ge₀.₃ supply layer at a doping density Of 2x10¹⁸ cm, a 3-nm undoped Si₀.₇ Ge₀.₃ spacer, and a 4.5 nm-thick Si₁₋ₓ,Geₓ channel graded from 0.8 to 0.7, and a 10 nm
Si$_{0.7}$ Ge$_{0.3}$ cap layer. The layer exhibited a 2-D hole-gas mobility shown in figure1.

\[ \nu = \mu F \]  

(3)

Where, \( \mu \) is the effective field mobility.

By the Shockley model equation describing the current-voltage characteristics of the MODFET at low drain to source voltage \( V_{ds} \) [4]:

\[ I_{ds} = \frac{\varepsilon \mu W}{(d + \Delta d)L} \left[ (V_g - V_{off})V_{ds} - \frac{V_{ds}^2}{2} \right] \]  

(4)

Where \( d = d_d + d_i \)
\( d_d \) = Thickness of the doped (B, SiGe) beneath the gate
\( d_i \) = Thickness of the undoped SiGe beneath the gate

In this expression one thing is noted down that \( V_g \) and \( V_{off} \) is negative because the device is 2-Dimensional Hole Gas.

\[ I_{ds} = \frac{\varepsilon \mu W}{(d + \Delta d)L} \left[ -(V_g - V_{off})V_{ds} - \frac{V_{ds}^2}{2} \right] \]  

(5)

The current is in ampere, and it is dependent to the length of gate and drain to source, so the dimension should be in account with length also, i.e. \( \frac{I_{ds}}{D_S} \), is the distance between drain to source.

Figure1: Modulation Doped Field Effect Transistor (MODFET)

Ids-Vds Characteristics of Modulation Doped Field Effect Transistor (MODFET):

Current–voltage characteristics of modulation doped field effect transistor may be found based on the charge control model, using the channel approximation concept, the surface carrier concentration in the channel is given by[3].

\[ n_s = \frac{\varepsilon}{q(d + \Delta d)} [V_g - V_{off} - V(x)] \]  

(1)

Where, \( x \) is the space along the channel length and \( V(x) \) is the channel potential equation.

The current through the channel is defined by

\[ I_{ds} = qn_s \nu(F)W \]  

(2)

The \( I_{ds} \) is the drain-to-source current, electron velocity \( \nu(F) \), which is the function of the electric field \( F \) in the channel. Here \( W \) is the gate width. Using the gradual channel approximation. The electric field in the channel is parallel to the heterointerface (it is directed from drain to the source) and neglect the diffusion current.

The electron velocity is simply proportional to the electric field:

\[ \nu = \mu F \]  

(3)

Where, \( \mu \) is the effective field mobility.

By the Shockley model equation describing the current-voltage characteristics of the MODFET at low drain to source voltage \( V_{ds} \) [4]:

\[ I_{ds} = \frac{\varepsilon \mu W}{(d + \Delta d)L} \left[ (V_g - V_{off})V_{ds} - \frac{V_{ds}^2}{2} \right] \]  

(4)

Where \( d = d_d + d_i \)
\( d_d \) = Thickness of the doped (B, SiGe) beneath the gate
\( d_i \) = Thickness of the undoped SiGe beneath the gate

In this expression one thing is noted down that \( V_g \) and \( V_{off} \) is negative because the device is 2-Dimensional Hole Gas.

\[ I_{ds} = \frac{\varepsilon \mu W}{(d + \Delta d)L} \left[ -(V_g - V_{off})V_{ds} - \frac{V_{ds}^2}{2} \right] \]  

(5)

The current is in ampere, and it is dependent to the length of gate and drain to source, so the dimension should be in account with length also, i.e. \( \frac{I_{ds}}{D_S} \), is the distance between drain to source.

Figure2: Ids – Vds characteristics for different gate voltages

The figure2 is current – voltage characteristics for different gate voltages. Here gate voltages varied from -0.5 to +0.5v.

When voltage at drain terminal i.e. \( V_d \) is applied then two
dimensional hole gas is accelerated by this voltage and current will flow because of lattice free charges are there so that it starts to flow a minimum voltage of $V_{ds}$ at negative gate voltage. In the figure it is clear that when gate is raised from negative value to positive values then graph is shifted to lower as shown in the figure 2.

IV. MOS-MODFET STRUCTURE

The processing of MOS-MODFET’s started with the deposition of a 20-nm-thick SiO$_2$ film using the JVD method [5]. To density the film, the sample received a post-deposition annealing at 300 °C in nitrogen ambient for 30 min. 240-nm-thick electron beam-evaporated SiO$_2$ film. The ohmic metallization of 30-nm-thick Pt was evaporated and lifted-off after the oxide in the ohmic area was removed by wet chemical etching. The gates length is 0.1μm with a trilayers resist system using electron beam lithography. Finally, the contact pads were defined by deposition of Ti/Pt/Au. The distance between source-drain is 4μm while the gate width of this device is 1μm. The device structure of MOS-MODFET’s is shown in Figure 3.

In the MOS-MODFET there is the slight change in the Height of the gate to channel distance. In MODFET the distance of the height is as ‘$d + d_i + \Delta d$’. But the MOS-MODFET the effected distance is counted as from addition of cap layer thickness i.e. ‘cap layer thickness + $d + d_i + \Delta d$.’

And formula is same as equation (5)

$$I_{ds} = \frac{\varepsilon \mu W}{(d' + \Delta d)L} [ (V_g - V_{off}) V_{ds} - V_{ds}^2 / 2]$$

Where $d'$ = thickness of cap layer + $d + d_i$

In this expression one thing is noted down that $V_g$ and $V_{off}$ is negative because the device is 2-Dimensional Hole Gas. So, the expression now slightly changes as:

$$I_{ds} = \frac{\varepsilon \mu W}{(d' + \Delta d)L} [ (V_g - V_{off}) V_{ds} - V_{ds}^2 / 2]$$

The current is in ampere, but the current is dependent to the length of gate and drain to source, so the dimension should be in account with length also. i.e. $\frac{I_{ds}}{DS}$ Where $DS$, Is the distance between drain to source.

Figure 3: Metal Oxide Semiconductors Modulation Doped Field Effect Transistor (MOS-ODFET)

Figure 4: Ids – Vds characteristics for different gate voltages

Ids-Vds Characteristics of Metal Oxide Semiconductor Modulation Doped Field Effect Transistor (MOS-MODFET):

In the MOS-MODFET there is the slight change in the Height of the gate to channel distance. In MODFET the distance of the height is as ‘$d + d_i + \Delta d$.’ But the MOS-MODFET the effected distance is counted as from addition of cap layer thickness i.e. ‘cap layer thickness + $d + d_i + \Delta d$.’
are there so that it starts to flow a minimum voltage at negative gate voltages current is higher than high gate voltages as shown in the figure4.

**Parameters Values Used:**

- Oxide thickness = 20 nm
- Thickness of Si$_{0.7}$Ge$_{0.3}$ cap layer = 10 nm
- Thickness of Si$_{1.4}$Ge$_{0.6}$ Channel graded 0.8 to 0.7 = 4.5 nm
- Thickness of Si$_{0.7}$Ge$_{0.3}$ Spacer = 3 nm
- Thickness of Si$_{0.7}$Ge$_{0.3}$ Supply layer B-doped 2 x10$^{18}$ cm$^{-3}$ = 4 nm
- Thickness of Buffer layer Si$_{0.7}$Ge$_{0.3}$ = 100 nm
- Thickness of Si$_{1.4}$Ge$_{0.6}$ Graded from x=0.5 to 0.3 = n-Si Substrate
- $\varepsilon_{SiGe} = 1.17 \times 10^{10}$ F/m, [6]
- $\mu$(for hole) = 815 cm$^2$/V-s
- Width of gate (W) = 1um
- Gate length (L) = 1um
- $\Phi_b = 0.9$ ev
- $\Delta E_c = 0.15$ ev
- $d_q = 4$ nm
- $d_i = 3$ nm
- $\Delta E_{eq} = 0.025$ ev
- $\Delta d = 9$ nm

### V. Conclusion

The MODFET and MOS-MODFET is novel devices in which channel are obtained by modulation doping as 2-DEG (Two dimensional electron gas) or 2-DHG(two dimensional hole gas). This channel is free from lattice scattering problems. The formation of oxide layer on to MODFET surface so, that there is a way to find CMOS devices. This device has better performance as Radio frequency range so its application in the wireless communication is very important as compared to other device in case of performance and cost effective.

### References


### BIOGRAPHY

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