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The Shift from Microelectronics to Nanoelectronics – A Review

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Abstract: In this paper a trend shift from the microelectronics to nanoelectronics has been discussed. Nanoelectronics is is the science which deals with the electronic components manufactured and engineered at a molecular scale. The electronics has been the main driving force for all the technological advancement taking place in the sciences. The research and development industry has presently been relying on the silicon based technology which was working at micro scale. The miniaturization of this technology is governed by the famous Moore's law. But with the advent in time, silicon based technology has reached its maximum limits of the reduction in size. Silicon encounters various physical and interaction problems due to which it cannot be used at a small scale of the order of nanometer. Hence this pushed the electronics towards the research of different materials which could be used at nano level. This paper talks about various candidate technologies that were approached for the purpose of miniaturization. It tells about the pros and cons for the every candidate technologies which were researched to succeed the throne of the present day silicon based technology. These nano materials suggested are smaller in size and exhibit properties of self assembly and self recognition. Hence this makes these nano materials to be used in the bottom to up nanotechnology technique.

Keywords: miniaturization, Moore's law, self assembly, self recognition.

I. INTRODUCTION

Moore's law could not be continued forever in the electronics industry. Gordon Moore, the co founder of the Intel, predicted that the number of transistors that could be placed on a chip would double every two years [1]. The various chip manufacturers have been relying upon this law for so long. By using this law they had achieved the exponential growth in transistor counts, but the scaling will end soon. The main obstacles are in the way: the limits of the lithography techniques, the rising cost of fabrication and the size of the transistor [2]. The use of the silicon in device manufacturing is going through the fundamental limitations including the tunneling current and the sub threshold current which lead to the high power consumption and circuit failure [3]. It was also observed that the contamination occurs during high temperature treatment of silicon [4]. Ultimately the goal of the scaling down process is to build an individual transistor which is smaller, faster, cheaper and consumes less power. Unfortunately, the scaling down of the lithographically patterned transistors could not continue forever, but the nanoelectronics may be able to continue this scaling down process. So before the discussion starts there is a small introduction to the metal oxide semiconductor field effect transistor (MOSFET). This would provide us with a better insight to understand the issues that complicate the scaling down process and provide a better contrast to the nano electronic device technologies studied afterwards.

II. MOSFET BASICS

MOSFET has been the major building block for the various computing devices over the decades. It is a four terminal device having the various terminals as drain, source, gate and the bulk (figure 1) [5]. In various digital circuits it is used as a switch. The source and the drain are the two ends of switch, while the channel is switched on and off under the control of gate voltage [5]. The MOSFET has been continuously scaled down to survive the Moore's law. Shrinking the feature size makes the transistor faster and consumes lesser power. The increase in speed is basically because of the decreased capacitance and increased current [5]. A first order approximation of the current across channel is given by the following equation 1 [6].

$$I_D = \frac{\mu C_{OX} W}{2 L} (V_{GS} - V_{TH}) \qquad (1)$$

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I_D is the current through channel, μ is the coefficient of permeability, C_{ox} is the gate oxide capacitance, W is the width of the channel, L is the length of channel, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage of the MOSFET.

Fig. 1: MOSFET diagram [5].

A. *Issues around Mosfet Scaling*:

The MOSFET scaling will soon come to an end. It has been shown that if the MOSFET is scaled down below 50nm, it has performance degradation. This is due to the loss of the charge in inversion layer with gate leakage and the degradation of the carrier mobility due to the increased scattering [7].

III. NANOELECTRONICS

After having known the physical and the fundamental limitations for the scaling down and the rising fabrication costs of MOSFET many researchers feel that the shift to the nanoelectronics would solve the problem. By mixing the fields of chemistry, biology, physics and the engineering a solution to the rising fabrication cost and scaling down process may be achieved. The largest change in a shift to nano-electronics is the method of fabrication. Individual wires, diodes, field effect transistors (FETs), and switches can be created abundantly and cheaply in a small setup. All of these devices would be so small that they may help reaching the smaller size integrated circuits (IC) which may not be possible with the conventional ICs. It is estimated that nanoelectronics will be able to integrate the devices at a much smaller level and that too by overcoming all the problems that prevail in the case of conventional ICs. In this paper the major research efforts for nano-electronics are considered by surveying proposed technologies for replacing the MOSFET in the present day technology.

A. *Technologies*

The devices used to build a circuit are the fundamental elements for any circuit. For the present day very large scale integration (VLSI) systems the silicon based transistors and copper wires are the fundamental elements. For nanoelectronics it appears that the silicon transistors and copper wires would be replaced by the nanoscale device technologies that have been discussed. The move to nanoscale devices is because they can be chemically developed at much smaller sizes than the conventional elements which can be patterned with lithography. There are innumerable technologies which can replace the transistor in may digital logic applications. They include carbon nanotube (CNT), Semiconducting Nanowire (S-NW), Quantum cellular automata (QCA), molecular electronic devices and graphene nanoribbon (GNR). These devices offer sizes of a few nanometers and could be self assembled. Figure 2 shows the schematic of various technologies that cover nanoelectronics.

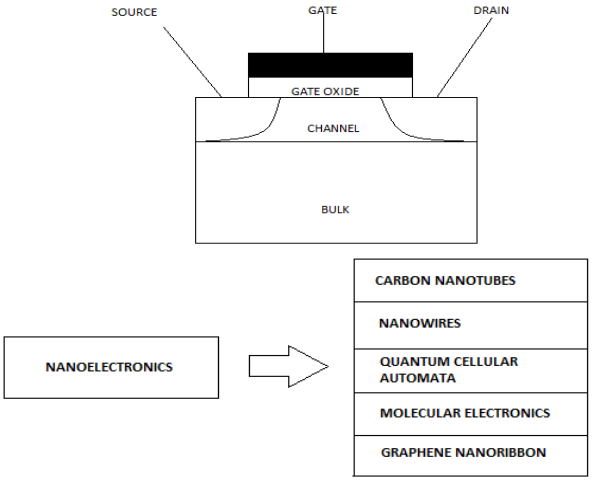

Fig. 2: The different technologies for nanoelectronics.

B. *Carbon Nanotubes*

These are the cylindrical arranged carbon molecules (figure 3) that exhibit unique chemical and physical properties, making them a good candidate in the nano-electronics [8]. Their structure gives the nanotube extraordinary strength which is attractive for the material use and also increases the durability of a nano-electronic circuit over the other materials [9]. Nanotubes can have varying properties which are dependent on the structure [10]. CNT were produced as a byproduct of an arc discharge experiment to create the carbon buckyballs [11]. CNT behaves as a metal or semi conductor depending upon the chirality. The chirality is the amount of twist present in the tube [12].A second property that affects the electrical characteristic of CNT is the number of walls [13]. The diameter of single walled carbon nanotube is about 0.7nm and that of multi wall carbon nanotubes is about 10- 20 nm [13]. The band gap energy is inversely proportional to the diameter [13]. So these CNT were used and tried for manufacturing the CNT based electrical devices like transistor. Figure 4 show the schematic of the CNT based FET. In this the silicon based channel has been replaced with the CNT. Most of the CNT transistors had been manufactured using the single wall carbon nanotube (SWCNT) because their band gap is in the range of semiconductor [13] [14] [15].

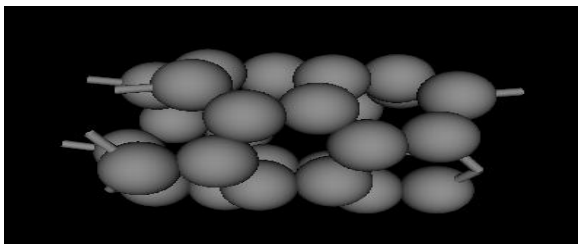

Fig. 3: Carbon nanotube structure.

One of the unsolved problems with the CNT is the fabrication problem. In CNT fabrication methods, they

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produce the CNT of both nature that is metallic as well as semiconductor [13]. These fabrication methods are not specific in nature. A method has been developed for this but it requires suspending the CNT into solution [16]. The

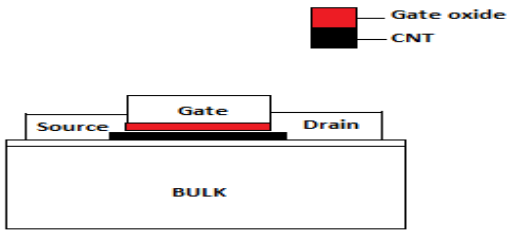

Fig. 4: Shows the CNT based FET.

chirality and width of the CNT is not under control during fabrication. So CNT could not fully replace the present devices.

C. *Semiconducting Nanowires*

These can be used as interconnect wires to carry the signals as well as active devices. Nanowires are long thin wires made up of the semi-conducting materials such as silicon or germanium that have been fabricated with a diameter less than 3nm [17][18]and a length of about few micrometers [19].Using the Semiconducting Nanowire (S-NW) various devices can be manufactured. For making the transistor we can dope the silicon wire in such a way that it has a small centre section in which the number of carriers are less, that is the low doping region is there [20].After this other S-NW is placed over the doped S-NW with an insulator in between to make S-NW based FET (figure 5) [21]. To make the pn junction join the p type S-NW with the n type S-NW to create a contact [22]. And hence p n junction is formed at a nanoscale (figure 6). The ability to grow the S-NW at a small scale hence makes them the important candidate for the nanoelectronics. Figure 5 shows the schematic of the S-NW based FET and figure 6 shows the schematic of the S-NW based pn junction.

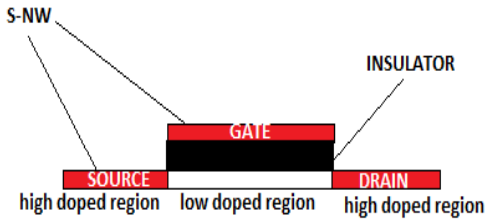

Fig. 5: Shows the S-NW based FET.

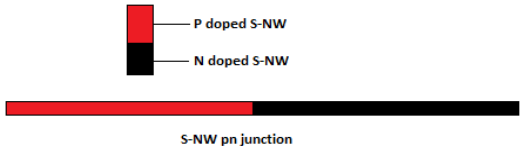

Fig. 6: Shows the S-NW based pn junction.

The problems encountered by S-NW at the nano scale are like there is a tunneling of the current, the sub threshold current increases the power consumption and the leakage of the current [3]. These are some of the unavoidable problems of the S-NW at the nanoscale level. Also the contamination occurs during high temperature treatment of silicon [4].

At the first glance it seems that CNT and S-NW are similar to each other. But there are some differences which make the S-NW better technology than CNT. The main problem with the CNT is to grow the CNT at a large scale according to the desired properties. The present day methods to make a metallic and the semiconducting CNT vary according to the tube. However in case of the S-NW these parameters could be easily controlled. The doping level can also be controlled in case of the S-NW whereas the CNT would either be metallic or semiconducting in nature.

D. *Quantum Cellular Automata*

It is a computational model made up of quantum dots. Basically a quantum dot encodes the information by looking upon the position of the electron [23]. It traps the electron by establishing a low potential region surrounded by high potential region. The nanometer quantum dots are constructed by using the aluminum by nano imprint lithography techniques [24]. The logic unit in quantum cellular automata (QCA) is the QCA cell proposed by the researchers at the University of Notre Dame. The QCA cell is composed of 4 or 5 quantum dots (figure 7) [23]. A quantum dot is a nanometer sized structure capable of trapping the electron. They are created by an island of conductive material surrounded by insulating material. Electrons which will enter the quantum dots will get confined over there because of the high potential required to escape. Figure 7 shows the basic QCA cell.

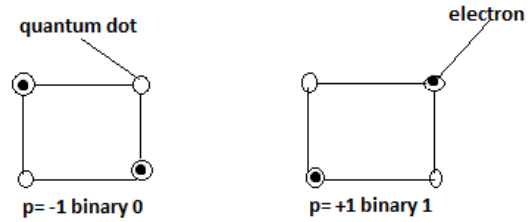

Fig. 7: Shows the basic QCA cell [23].

In figure a basic logic decision for 1 and 0 has been shown by using the QCA cell structure. It gives the basic decision of the 1 and 0 by making use of the relative position of the electrons inside the quantum well [23]. So this basic QCA cell can be used to realize various logically operating devices and can replace the conventional microelectronics.

E. *Molecular Devices*

Even though CNT, S-NW and QCA cell can be used as active devices as well as wires in nanoelectronics, there is also a set of molecules that could be used as the active

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devices. These molecules behave as diodes or programmable switches that can make up the programmable connections between wires. Chemists have designed these carbon-based molecules to have electrical properties similar to their solid-state counterparts. Molecular devices have one huge advantage over solid-state devices: their size. Thousands of molecules can be sandwiched between micro-scale wires to create an active device that takes up very little area. Present VLSI cross points made of pass transistors are 40-100 times larger than a wire crossing or via [25]. Since molecular devices fit between the wires, large area could be saved. It has been estimated that the use of S-NW and molecular switches could reduce the area of an field programmable gate array (FPGA) by 70% over a traditional SRAM based design at a 22nm process [26]. In addition to being very small, molecular electronic based devices are nonvolatile. The configuration of the molecules remains stable in the absence of electric field. In the presence of electrical stimulation, programmable molecular device can be turned on and off which can be used to perform logic. Molecular diodes, molecular switches, single electron transistor are some of the products that molecular electronics has given us.

F. *Graphene Nanoribbon*:

In this process of scaling down the scientists found a new material named graphene which had very good properties and had shown a ray of hope to be used as a replacement material for the silicon. So since then Graphene has been regularly discussed and has been investigated extensively to help produce a new generation of the electronics. Basically graphene is a material made up of carbon atoms arranged in 2d honeycomb lattice and can be utilized to make the various other carbon based materials, namely carbon Bucky-ball structure, carbon nanotubes, graphene nano-ribbons and the graphite [27]. Carrier mobility from 3000-15000 cm^2/Vs can be achieved even under ambient conditions, which makes it an important material for use in nanoelectronics [28] [29]. Also it was further known that the carrier transport in graphene takes place in π-orbitals perpendicular to the surface [30]. So in the structure this translates into a mean free path for carriers of L = 400 nm at the room temperature [28]. Hence it makes the ballistic transport possible even at the scaled down device compared to the CMOS technology at present. An added advantage in graphene is that the electronic transport follows the Dirac equation and the charge carriers are relativistic in nature [31]. Also the carriers have shown to be having zero effective mass and travel at the speed of light which makes the use of graphene into the devices more favorable as they will work at higher speed [31]. However the use of the graphene in the digital based applications was not made because that it lacked the energy band gap. Thus, in spite of having high carrier mobility and significant current characteristics the graphene could not be used in digital applications because the conduction in graphene could not be switched off due to the absence of band gap. In the mean time some research workers were able to propose a bilayer graphene complementary field effect transistor [32]. This showed high on/off ratio making an important step towards graphene based logic devices [32]. One of the ways to open the band gap is patterning the graphene sheets into narrow ribbon [33]. Scanning tunneling microscope (STM) lithography is the process by which an energy gap can be introduced in a precise manner, turning the metallic graphene into semiconductor [33]. The energy band gap is inversely dependent on the width of the graphene nanoribbon [34]. So by tuning the width of the graphene nanoribbon we can get the desired energy band gap. By cutting the graphene sheet into different length and width we can create the graphene nanoribbon (GNR). This nanoribbon can further be utilized to replace the interconnects because of their high carrier mobility's and other exceptional properties. Also we can use the GNR of different types to form a graphene field effect transistor (GFET). The proposed graphene nanoribbon (GNR) device has the electrodes part made up of zigzag graphene structure, that is metallic in nature and the central portion, which acts as a channel or conducting portion, is made up of semiconducting arm-chair shaped graphene. The 3 terminal device as shown below (figure 8) could be formed which is gate enabled and hence can work as a replacement for the present day transistor. Figure 8 shows the schematic diagram of the G-FET device.

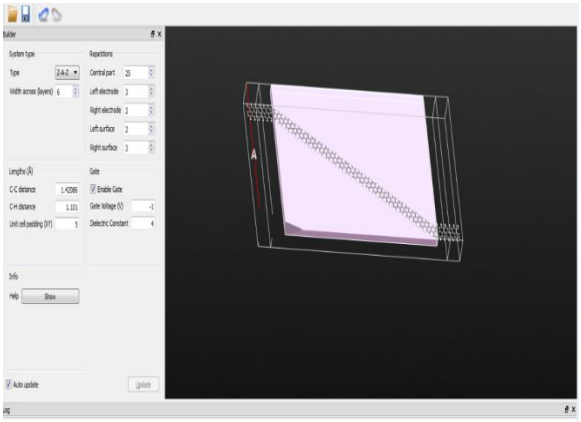

Fig. 8: Shows the G-FET device.

IV. CONCLUSION

The future electronic circuits are getting smaller but there is no compromise with their performance. The CNTs, S-NW, QCA, molecular electronic devices and graphene nanoribbon could easily replace the conventional microelectronics and lead to the miniaturization of the integrated circuits (IC). This will be huge leap in technology which will use small size electronic components and lead to increase in the density. The need of hour is to model robust methods for fabrication processes that can be used to process these advanced technology devices at a larger scale. Attaining control over the interfaces of these devices would further

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help in creating nanoscale integrated circuits. This achievement would pave a path towards interfacing nanoscale electronic devices with ultra-dense integrated circuitry. Table 1 gives the summary of different nanoelectronics techniques.

TABLE 1: SUMMARY OF DIFFERENT NANOELECTRONICS TECHNIQUES

Technology	Size	Fabrication	Lithography	Problems
CNT	Few nm	Complex	STM	Fabrication problem
S-NW	Few nm	Simple conventional technique	Conventional technique	Tunneling of current and subthreshold current
QCA	nm	Simple	Nanoimprint	Applicable in logic devices only
Molecular Device	nm	Complex	STM	Pratical implementation
GNR	Few nm	Complex	STM	No problem

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