ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 10, October 2013

An Overview of Implementation of Efficient QRS Complex Detector with FPGA

Priyanka Mundhe[1], A.K.Pathrikar[2]

Student, Electronics, Savitribai Phule Women's Engineering College Saharanpur Aurangabad, Maharashtra, India[1]

H.O.D, Electronics, Savitribai Phule Women's Engineering College Saharanpur Aurangabad, Maharashtra, India[2]

Abstract: Electrocardiograms (ECG) have become one of the most important, and widely used medical tools for diagnosing diseases such as cardiac arrhythmias, conduction disorders, electrolyte imbalances, hypertension, coronary artery disease and myocardial infarction. QRS is the dominant complex in the Electrocardiogram (ECG). Its accurate detection is of fundamental importance to reliable ECG interpretation and hence QRS detection is an important part of many ECG signal processing systems. In this paper we proposed an efficient architecture for implementation of ECG QRS Complex Detection algorithm. In this proposed system Real time ECG database is taken as input and baseline wondering and background noise are removed from ECG signal by using mathematical morphology. Simulation of the algorithm is done by using XILINX ISE simulator. The whole architecture is implemented in XILINX VIRTEX 5 FPGA.

Keywords: ECG, QRS Complex Detection, baseline wondering, XILINX, FPGA etc.,

1. INTRODUCTION

An ECG (electrocardiogram) is a test that measures the electrical activity of the heart. In an ECG test, the electrical impulses made while the heart is beating are recorded and usually shown on a piece of paper. This is known as an electrocardiogram, and records any problems with the heart's rhythm, and the conduction of the heart beat through the heart which may be affected by underlying heart disease. An ECG consists of P wave, QRS Complex and T wave Out of these characteristics QRS Complex is very important[7] and its accurate detection is required. The good performance of computerized ECG processing systems relies heavily upon the accurate detection of the QRS complex. Many sophisticated algorithms have been proposed to improve the accuracy of QRS Detection. Three different classes of algorithms for the automatic detection of this complex can be found in the literature. Non-syntactic, syntactic and hybrid .The main advantage of the syntactic methods is focused on their ability to use the structural information of the ECG signal and describe more complex relations than the common non-syntactic methods. However the computational cost of these methods is in general high. The average complexity is equal to the time complexity of a context free grammar (CFG) parsing. non-linear transforms. a specific QRS template which might be considered the best way to prevent the QRS detection performance from being degraded by the undesired noise sources.

The above fig.1 shows a novel computing method devised based on simple moving average combined with wavelet-based denoising for real-time QRS detection is introduced. Among these, some algorithms were developed based on digital filters in order to extract the feature Components due to the QRS complex; some were based on QRS complex is varying with the physical variations and also affected by noise as time evolves. Therefore, seeking for a reliable QRS detection algorithm is essential to the realization of automatic ECG diagnosis.QRS is the dominant complex in the Electrocardiogram (ECG). Its accurate detection is of fundamental importance to reliable ECG interpretation and hence, to all systems analysing the ECG signals (e.g. Heart-monitoring).Syntactic methods are a very powerful tool for QRS detection, since they can easily describe complex patterns, but their high computational cost prevents the implementation for real time applications. In this paper, we present VLSI architecture for ECG signal processing. The corresponding VLSI architecture is designed and implemented on a commercial nano-FPGA. The good performance of computerized ECG processing systems relies heavily upon the accurate detection of the QRS.

Fig.1. Block Diagram of QRS Detection

In this method, the DWT [2] is computed in an efficiently real-time manner using the recursive pyramid algorithm (RPA). The real-time implementation of RPA requires significantly smaller memory storage, as compared that

ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 10, October 2013

required by the direct computation of DWT, and thus permits a memory-efficient computational architecture of DWT. Also, the proposed method employs a simple moving average filter for extracting the QRS feature from the denoised ECG data so the number of operations, i.e. multiplications and additions, required is less than that for most of the existing algorithms, thus allowing a simple and time-efficient realization of real-time QRS detection, either in software or in hardware manners.

II. QRS Detection Algorithm

There are many QRS Detection algorithms which are mentioned above out of these algorithms we exploit the pan and Tompkins QRS detection algorithm and provide low power architecture for that .Pan and Tompkins[3] propose a real time QRS Detection algorithm based on analysis of the slope, amplitude and width of QRS complexes. This algorithm includes series of filters and methods that perform low pass, high pass, derivative, squaring, integration, adaptive throsholding and searcg procedure. Below figure illustrates the steps of algorithm in schematic form.

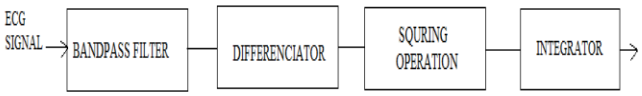

Fig2.Block Diagram of Pan-Tompkins Algorithm

For a homecare ECG monitoring device, it is important to extract the features of the ECG signal in real-time. The ECG feature such as R-R interval, QRS amplitude and duration, the magnitude and duration of **p** wave, potential of **S-T** segment , and the magnitude and duration of **T** wave are important for homecare applications. For example, the information or feature of **R-R** interval can be derivate to analyze the heart rate variability (HRV). The duration of QT interval can be used to determine the status of myocardial re-polarization. The objective here to report successfully development of a real-time ECG QRS detection algorithm that could be implemented using Field programmable Gate Array (FPGA) device with low power. The implemented System on Chip (SOC) using FPGA

that could be used to acquire digital ECG data from an Analog-to-Digital Converter (ADC), to display ECG and extracted information on a VGA type LCD device, to store the acquired ECG and the extracted information into a flash memory chip and to communicate to a PC computer using an USB device. The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL).Simulation is performed in XILINX ISE simulator and implementation is done in *Xilinx 9.2* with Virtex device.

III. METHOD FOR PROPOSED SYSTEM

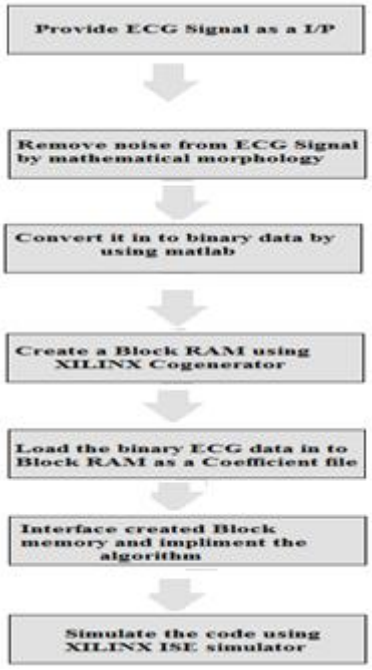

Fig.3.flow chart of real time simulation

The above figure shows the Real time Simulation setup for the proposed system. The algorithm will be analyzing the component of the ECG signals and information in real time for identifying the abnormal rhythm and heart beat. The programmed System on Chip (SoC) will be controlling the detection and digitizing ECG, analyzing and extracting feature of ECG, monitoring the information update to the LCD, interfacing with USB and Flash Memory. In this way, both the ECG signal in real time and the analyzed information can be displayed on the LCD panel. The information can be transmitted and presented using self-developed software that is designed with Borland C++ Builder through USB device. The ECG data from MIT-BIH database could be input from hosted PC to the prototype system by USB bridge device. The real-time ECG acquired and digitized data could be input to the prototype system directly.

IV. POWER REDUCTION TECHNIQUE

There have been a number of power reduction methods that have been used for some time. Some of them are Clock gating, Gate level power optimization, Multi-VDD, Multi-VT etc. The method employed by this paper for power reduction of ECGQRS detection blocks is clock-gating [6]. A significant amount of dynamic power is consumed in the distribution network of the clock. This happens because the clock buffers have the highest toggle rate in any circuit. In addition, the flops receiving the clock dissipate some dynamic power even if the input

ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 10, October 2013

and output remain the same. A simple solution to this power consumption is to turn off the clocks when they are not required. This approach is known as clock-gating.

V. FPGA Architecture

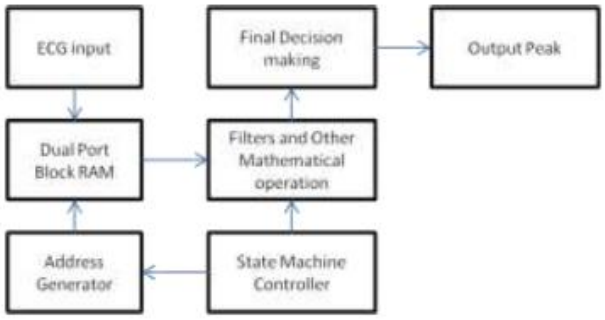

Fig.4. Architecture of the Logic

The ultra-low power consumption is essential for ECG The design strategy of the hardware implementation is to reduce as much computation load as possible and the power requirement as in FPGA power consumption is less [8].

I. CONCLUSION

The various applications of ECG signal and various QRS Detection algorithms are presented and have been studied in this paper also a novel approach for the implementation is given. The main objective of this paper is to implement the QES detection algorithm by using FPGA so is occupies less area and low power.

ACKNOWLEDGMENT

I express my sincere gratitude and indebtedness to my guide Prof. A.K. Pathrikar for his initiative in this field of research, for his valuable guidance, encouragement and affection for the successful completion of this work. His sincere sympathy and kind attitude always encouraged us to carry out the present work firmly. I express thankfulness to Principal Dr.G.S.Sable. for providing us with best facilities and his timely suggestions.

REFERENCES

[1] Chris F. Zhang and Tae-wuk, Bae "VLSI Friendly ECG QRS Complex Detector for Body Sensor Network" Vol 2,No.1March 2012
[2] F.Zhang &Y.Lin "Novel QRS Detection by CWT for ECG sensor"in proc.int.conferenceIEEE Biomedcircuit system montrael Canada nov 2012.
[3] J. Pan and W. J. Tompkins, "A real-time QRS Detection algorithm,"IEEE Trans. Biomed. Eng., vol. 32, no 3, pp.
[4] B. U. Kohler, C. Hennig, and R. Orglmeister, "The principles of software QRS detection," IEEE Eng. Med. Biol. Mag., vol. 21, no. 1, pp. 42–57, Jan. 2002.
[4] S. Kadambe, R. Murray and G. F. Boudreaux-Bartels, "Wavelet transform-based QRS complex detector,"IEEE Trans. Biomed. Eng., vol. 46, no 7, pp. 838-848, Jul. 1999.230-236, Mar. 1985
[5] Y. Yoshida, B.-Y. Song, H. Okuhata, T. Onoye, and I. Shirakawa, "An Object Code Compression Approach toEmbedded Processors", ISLPED-98: ACM/ IEEE International Symposium on Low Power Electronics and Design, pp. 265– 268, Monterey, California, August 1997.
[6] M. Pedram, "Power Minimization in IC Design: Principles and Applications", ACM Transactions on Design
Automation of Electronic Systems, vol. 1, no. 1, pp. 3–56, January 1996.
[7] K.P.Birman "Rule Based Learning for more accurate ECG analysis" IEEE Trans.patt:March intell pp 369-380 1982.
[8]Y. T. Chiang and K. S. Fu, "Parallel parsing algorithms and VLSI implementation for syntactic pattern recognition," IEEE Trans. Pattern Anal. Mach. Intell., PAMI-7, no 3, pp. 302- 313, 1985.

BIOGRAPHIES

Priyanka Mundhe, is student of ME Electronics from Savitribai Phule Women's Engineering college Aurangabad

A.K.Pathrikar is firmly assistant professor & H. O.D of electronics in Savitribai Phule Women's Engineering college.His qualification ME (Elecronics).His major areas of interest are VLSI, Microwind and signal proceesing.