ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 11, November 2014

Performance Analysis of Boostable Repeater in Different VLSI Interconnects and Applications

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Abstract: In the era of Nanometer technology variation of process aging of circuits cause vulnerable to establish circuits with the characteristics of adapting themselves and thereby a chance to compensate changes with the proposed one. Aging of circuitry and variations in process are main problems to analyze the efficiency of power circuit interconnects as a adaptability of power requirements must be assigned to drastic timing variations. The allocated design time implies uniform consumption of power on several fabricated chips, even of many circuit instances do not have considerable changes. This proposed design produces an efficient approach for power to tolerance variations. Hence it uses only power when the variation circumstances of a chip circuit instance are being harmful.
The proposed is an effective work towards adaptation of power supply voltage for changing resilience in VLSI chips. This proposed is a repetition based boostable design that can unanimously raise its internal potential rail to increase circuit switching speed. This Modality can be either ON/OFF to compatible power fluctuations. This repetition based boostable design enhances fine scaling voltage adaptation with voltage regulators. Since inter connections of a circuit is a widely available cause in chip performance and several repeaters are provided an IC designs, this repetition based boostable circuit has large number of tips to improve system performance.

Keywords: Interconnects, Process variations, switching time.

I. INTRODUCTION

The Present Technology has significant impact with process variation this is because as shrink of technology continuous the negative Impact on performance and power consumption. Die allows post tuning changes with respect to device deviations during manufacturing. As the transistors and clock frequencies are increasing in a die it has been major concern for a microprocessor about power density. Circuit aging and process variations are major difficulties observed in a nanometer process still there are concerns on efficiently reducing variation effects. By using large guard bands the performance requirements can be satisfied. However wastage of substantial resources and design overhead are related to power which affects the process variations. Therefore there is a need of fundamental strategy to reduce process variations. This work is an effort to provide adaptive design for above said effects. Adaptive design of a circuit has change in two components majorly such as detection and compensation. This happens due to variations in the design circuit and also yields in complexity.
To achieve high switching speed and very low leakage in power a voltage is to be tuned at threshold level. The tuning range can be limited to forward bias junction as ABB can be used for fine granularities with little overhead and this level will be sustained with present technologies. As technology is growing power performance tuning is having more concentration this can be achieved by bringing the voltage to adaptation level. Usually the adaptation level of voltage highly depends on granularity by using off chip regulators of voltage major building blocks which can be achieved in coarse grained. This can reduce the overhead and the effectiveness in compensation of voltage regulators.
Fine granularities have voltage variation effects, In order to understand this consider two neighboring transistors having doping fluctuations and switching activities which result in aging and variation effects considerably. As voltage is increased to last level some of the paths have same block but some deviations provide wastage of power. Power grid or network has more effect produced by Fine grained voltage adaptation. To reduce large overhead if voltage tuning is applied to hundred gate blocks then ten thousand voltage regulators are required which is almost impossible. So it is difficult to work with less number of gates in million gate chip.
Voltage regulators can be reduced by choosing any line of VDD parallel from a circuit block as supply. This can be done only when the size of block circuit is small. Modern world supports chip designs which have power grid and additional overhead and huge complexity.
By using high voltage rail speed can be improved which is used in boostable repeaters. This dual VDD buffer and extra load to timing path does not have effect on boostable repeater design. This ABB design uses fine grained adaptation and resilience to variations for efficiency in power. The overhead of timing paths is less in ABB and has small effect on overhead area. To reduce area overhead boostable repeaters are arranged in small number. The variations can be reduced also by using a supply voltage tuning which is a global tuned. One of the problems seen in ABB design is guard bands pessimism. This can also be reduced somehow by tuning equip circuits on its own. This is to focus on developing both variation detection and compensation techniques in order to provide a complete adaptive system. Various existing adaptive approaches will be reviewed and their limitations

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
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to fine grained variation compensation will be analyzed as well. To effectively address the limitations, the proposed voltage and frequency adaptation techniques, use area-efficient delay variation detection scheme. Interconnect in chips is done by using wires, stick diagrams, Transistors these elements constitute as layers of wires which run orthogonally as they have power, speed and noise in alternating layers. To change from quadratic to linear delay dependency the possible answer is to have repeater insertion.

In Interconnect synthesis work sizing tools and repeater insertion is used in delay dependency. Driving interconnect load can be done by choosing optimum number of repeaters and their corresponding sizes. By using repeater models and increasing the resistance of repeater the strength of repeater drive can be increased and overall delay can be reduced. This approach or idea is advantageous in deep submicron process as drive strength is increased by increasing the interconnect resistance. The repeaters used provide propagation delay as they are individually used in reduction of delay. Direction of repeater is also a factor in conventional repeaters which should be appropriately done otherwise it cannot be used in conventional repeaters.

High performance in boostable repeaters is done by tuning the circuits as on or off. It can be used in dynamic power management by programming online. Interconnect is an important element in deciding the performance with repeaters which is used in plenty. Boostable repeater uses adaptive system to compensate variations in fine grained. VDD low gives a adaptive value to avoid degrading critical paths by meeting real time constraints.

II. LITERATURE SURVEY

A. Existing Methods

The approaches of variation compensation are given by Body Bias Voltage and Supply Voltage. By changing the body biasing, then the V_t is varied, If this effect is more body bias voltage is lower V_t of transistor and higher V_t to reduce reverse leakage power. Supply voltage sometimes is known as Adaptive Supply voltage (ASV) which is compensating changes in Power supply. ASV is having several features compared to body bias voltage (BBV). Therefore, Very firstly ASV is used for all types of circuits where BBV is applied for SOI circuits. And the second one is leakage power and Dynamic Power Dissipation

The leakage power (PLEAK) and dynamic (switching) power (PD) can be expressed as,

$$P_{leak} = I_{leak} \cdot v_{dd}$$
$$P_D = \propto f C v_{dd}^2$$

where I_{LEAK} is leakage current of a given circuit α is proportional factor f is frequency constant and C_l is capacitive load.

B. Abrupt changes of Adaptive Supply Voltage (ASV)

ASV reduces dynamic power dissipation by tuning power supply voltage. ASV is stronger than BBV. The Nanometer technology having fine grained process variations. To distinguish transistors we have different Rubylith variations and different doping possibilities and the switching activities of any two transistors is also different.

From these fine distinguishing are combining together there is a possibility of several critical delay paths are present which are providing instability for ASV. Then this supply voltage is increased in few delay paths. Then an extra power supply is read for these paths without any variations and this power is wasted.

C. Dual Static power supply rails

Currently, Dual static power supply rails based techniques are appeared they provide that two power supply rails (V_{DD}) are required to the block of a circuit. This circuit block is connected to either low or high VDD through transistors which are in sleep mode. The change between two power supplies is so small then there is no change necessity of level shifters for power supply rooms. These effects do not provide details on how to find the two different supply voltage rails at the place which is very difficult when the sizes of different blocks are less i.e., This approach provides nearly two time s of power grid nets. Power grid in current circuit designs is bulk in size and has limited circuitry for additional effects.

D. Discussion on generation of power Supply Voltage

Fine scaling ASV and dual static power supply rails requires more than one power supply. From this it can be considered as only two options to provide required power supply

Option 1: Generate power from an external voltage regulator and transfer it to internal destinations.

Option 2: Generate power from locally used internal voltage regulators

These voltage regulators are of two types switching regulators and linear regulators. Linear regulator is complex to analyze and very easy to placed internally and has very quick response. However its efficiency of energy is less compared to switching regulations. When potential difference between power supply input which is regulated is huge. Switching regulators can be classified in to two types mode switching regulator and capacitor switching converter.

For dual power supply static rails if one having the additional potential through option 1 there will be huge power delivery circuits due to supply lines which are duplicated.

E.Proposed Work

. The proposed work is a design of boostable repeater to evaluate the performance of the design circuits to find the variations in processes. The design can be transiently switch unanimously to raise the voltage rail internally to find out the switching speed. Design of Boostable repeaters is to achieve voltage adaptation to fine grained circuits without disturbing the supply voltage regulators.for tolerance change there is an adaptive design which is very efficient in saving power. The work design is greatly modified by reducing the overhead in the control circuit. This functionality disables or enables the according to the boosting function. This change can be obtained by detecting the variations in circuit process The

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
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objective of this work is provide more efficiency in power for VLSI circuits. The main idea is a boostable repeater design that can transiently and autonomously raise its internal voltage

rail to boost switching speed. The boostable repeater design achieves fine-grained voltage adaptation without stand-alone voltage regulators or an additional power grid. Adaptive design provides a power-efficient approach to variation tolerance.

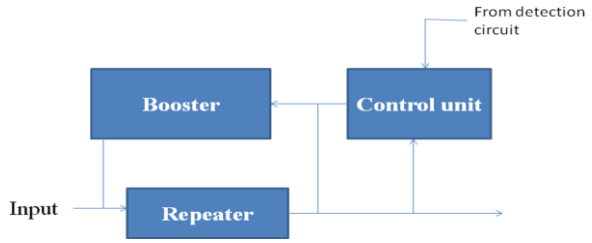

Fig. 1 Shows the Proposed work details with neat schematic

The Further simplified version of the circuit can be seen as below

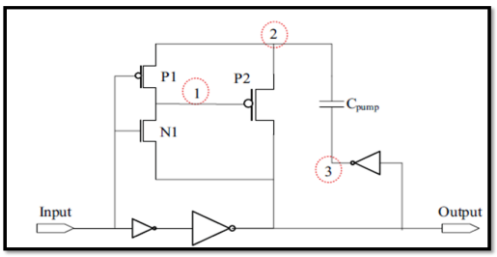

Fig. 2 shows how the input is processed with boostable repeater logic

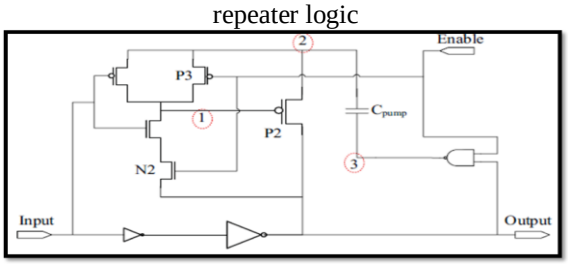

Fig. 3 shows in detail view of the block schematic

The design can be greatly simplified and the overhead can be largely reduced. The control circuit activates or disables this boosting function according to an "enable" signal, which is usually obtained from variation detection circuit. Process variations and circuit aging continue to be one of the main challenges to the power-efficiency of VLSI circuits.

III. BOOSTABLE REPEATER DESIGN

To provide fine grained circuit the repeaters should be adaptive where the design of adaptive repeaters is controlled to operate in low power mode or high performance.

The proposed work transiently switches from high static supply to support VDD in achieving high performance under high voltage. This mode is similar to conventional circuits.

The design is followed with 4 capacitors of 2 Pf fixed value and the layout used is double poly capacitor. The typical frequency is 4.5 to 5 Mhz and quality factor is 250.

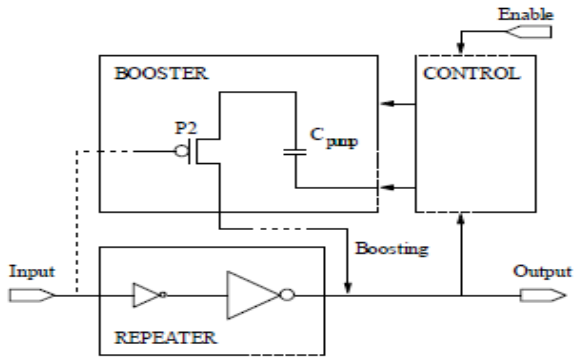

Fig. 4 shows schematic view of boostable Repeater

A. *Design and Operations*

The design of Boostable repeater is involved in the principle of ON and OFF and describes the operation in two conditions i.e., when it is ON and when it is in OFF

B. *Boosting On*

If the boosting feature is always on and cannot be turned off, i.e., it is not programmable, the design is a simplified version shown in Fig. 3.2(a). Transistor P2 is the pass transistor that delivers current from Cpump to the output node. Transistor P1, N1, and the inverter between the output and node 3 coordinate the operations. The operations mainly include two phases: charging and boosting. : Always the boosting feature is in ON condition and it cannot be off condition. Hence it can be said it is non programmable. The schematic view in a simple manner can be seen in Fig 3.2(a) the transistor p2 is a element which provides the current from Cpump to output terminal node. The total operation depends on the inverter and between node 3 and output terminal and transistor P1, N1. This boosting condition in ON presents two phases which are boosting and charging.

C. *Charging Phase*

The capacitor Cpump is charged only when input and output are present in stabilized condition to high or VDD. Fig 3.3 describes the waveforms of phase operation, usually when the input and output becomes high p1 is in off condition and N1 is on condition and voltage node v3 is at low. Since N1 is 0V and node 1 voltage is VDD-Vt,n where V t is the threshold voltage of V1. VDD at the output node 2 is passed through p2 where the pass transistor is ON partially. Therefore it can be shown that Cpump is charged.

The Cpump potential is noted as the difference between v2 & v3 . this Potential is observed during the charging phase where the potential of v2 & v3 increases. VDD is increased by Cpump this happens then both input and output are switched low.

When the output is low:

This condition when the inverter goes high with increase in V3. The potential difference of Cpump will be the same. In the next condition as V2 increased beyond VDD.

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
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The value v2 is about 1V which is very much greater than Vdd 0.9 V. If the input is low N1 is switched in to off condition and p1 is ON Then this element connects node1 and node 2 in which p1 and v1 values which follows the same potential of v2.
Similarly as the node is not connected to any output node the p2 is switched to off condition. With this calculation it can be seen that both V1 and V2 will reach 1V at 0.4 ns time.

D. Boosting Phase

This situation happens when switching rise time of input increases. The waveforms can be observed in figure 3.
Because of switching gate transistors of input and output the time period is very short and output is drastically very low as the input goes high also. The time period at this instant makes N1 is ON and makes the V1 to low.
The boosting starts where there is a very low potential at node 1 and switches to ON as the P2 pass transistor and Cpump discharges and provides pull up at the output.When this happens there is a rise at the output which is pulled at the output by the VDD.
This transistor accelerates the boosting and provides very high rise with increase in the switching speed. Because of area overhead and pass transistor p2 the cpump capacitor is shown by trench cap. This provides the efficient area the difference in sizes for P1 & N1 and inverter, between the output and Cpump are switched. Therfore the extra load capacitance effects the system.

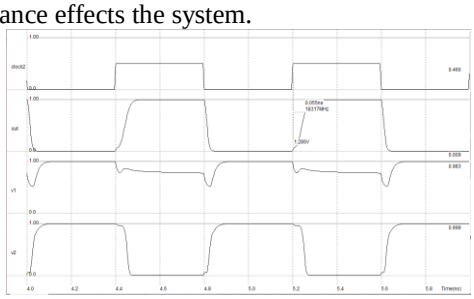

Fig. 5 Charging and boosting phases of Boostable Repeater.

E.ASV system in Dual Level:

A sophisticated adaptive supply voltage (ASV) system is proposed for delay critical paths and timing circuits. This flow design is reduced to provide very less delay in critical paths and non critical paths of resistor power The delay in path is made equal by using same timing constraints. This mechanism provides a broad range of chances in induced variation with timing factor from less paths to more paths. This wide range makes ASV very difficult to implement. If one adopts coarse-grained ASV, there could be considerable power waste when the degradation actually occurs only on a few paths. If one chooses fine-grained ASV and prepares for degradations on many paths, a large overhead on power routing or voltage regulators is usually incurred.Our system solves the aforementioned difficulty by simultaneously providing coarse-grained and fine-grained ASV. In this dual-level ASV (dual-ASV) system, power routing overhead is largely avoided by a new technique of voltage tapping in the context of voltage island based designs. It is also considered the impact of the variations on the dual-ASV system embedded in the circuits. The results indicate that our approach can achieve similar performance and robustness with significantly less power dissipation. The average power reductions are 40% and 21% compared to over-design and conventional ASV, respectively. A weakness of our approach is that it is limited to voltage island based designs.However, multi-supply-voltage designs become increasingly popular for the sake of power management. Therefore, the limitation of our approach will become less severe.Overview and detailed implementation of the proposed dual-ASV system, and its corresponding analysis and verification will be presented.

F. Boostable Repeater for Variation Tolerance in Interconnects

In this work, we propose a new approach for fine-grained voltage adaptation boostable repeater, which can boost its switching speed through transiently and autonomously enhancing its internal voltage rail. The boosting feature can be turned on and off at runtime and therefore can adaptively compensate delay variations. It does not require voltage regulator or additional power grid. Since its adaptively is per repeater, it is inherently fine-grained.
A previous technique in the same direction is online adjustable buffer (OAB). Roughly speaking, an OAB is a static CMOS buffer augmented by a tri-state buffer in parallel. The tri-state buffer is turned on (off) when the OAB operates for high-speed (low power). In order to significantly reduce delay at high-speed-mode, the size of the tri-state buffer needs to be close to that of the static CMOS buffer. This means that an OAB at low-power-mode has intrinsic load of twice as much as that of a single static CMOS buffer. In other words, this technique improves one mode at the cost of degrading another mode.
Unlike OAB, which relies on dynamic device sizing, our boostable repeater exploits transiently higher voltage rail for speed improvement. Therefore, the extra load presented to timing path from a boostable repeater is significantly smaller. Another related work is dual-VDD buffer. However, it requires two VDD lines like. The boostable repeater design enables fine-grained circuit adaptation and therefore power-efficient resilience to variations. It presents limited load overhead to timing paths and thus has small timing penalty in low power mode. The weakness is that it has significant device area overhead.
This is because we propose boostable repeater to compensate fine-grained variations, in other words, severe degradations on a limited number of critical paths. In conjunction with ASV, we maintain global VDD low while significantly degraded paths can still meet their timing constraints with the boostable repeaters. The proposed adaptive system with boostable repeaters integrated with global ASV system is validated through SPICE simulations on various test cases. Compared to ASV alone, our approach achieves an average of more than 25% power reduction with the same performance and robustness.

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International Journal of Advanced Research in Computer and Communication Engineering
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IV. DESIGN IMPLEMENTATION

Some of the design preferences should be observed are basic and conventional repeater, Boostable Repeater, Width-single cell, Layout editors (CAD) tools, 32 nm. Two Important design parameters have major impacts about size of the pass transistor P2 and Cpump capacitor. This effect can be seen in the form of dotted line where width of P_2 or C_{pump} increases the speed is boosted of designed repeater increases.

A. Design Parameters

To provide high speed the voltage v2 at node 2 is increased where the difference is shown in solid line the curve at the right shows the increase of v2 and gained speed which automatically consumes more power. Therefore this waveforms or curves help in choosing sizes of C_{pump} and P_2

The width that is generally employed is 1.7µm for the pass transistor p_2 and the Capacitor used C_{pump} 10fF

B. Software Requirements

For simulating the carried work Micro wind 4.0 is chosen which gives a design schematic with various layout editors. The basic requirements are given below

1. Microwind 3– CAD tool
2. 32 nm layout editors
3. 32 nm layout analysis tool

The simulation and design of CMOS integrated circuits can be easily done by using Micro wind 3 PC tools.

The lite version of these tools only includes a subset of available commands. The Lite version is freeware, available on the web site www.microwind.org.

V. SIMULATION RESULTS

The simulation results involve the design of conventional repeater and boostable repeater describing the waveforms for different length and width between voltage, time and current. These results show the working functionality of these repeaters for various layout editors.

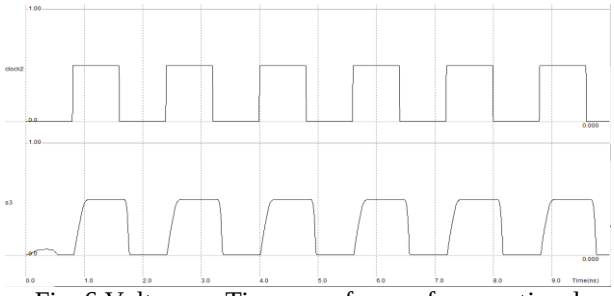

Fig. 6 Voltage vs Time waveforms of conventional repeater at length & width 70 & 140nm

The Fig 6 shows the voltage versus time waveforms of conventional repeater at length & width of 70 & 140nm. Clock2 signal is input and S3 is output of conventional repeater. The conventional repeater repeats the voltage at input end. Here we get the output S3 is approximately equal to the input signal.

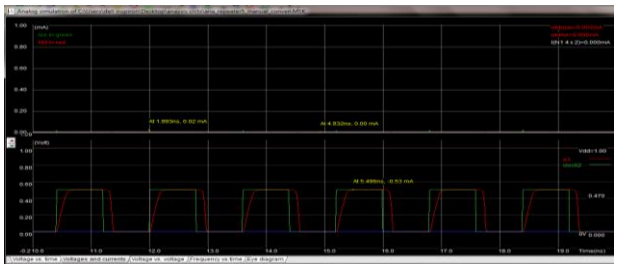

Fig. 7: Voltage vs Current waveforms of conventional repeater at length & width 70 & 140nm

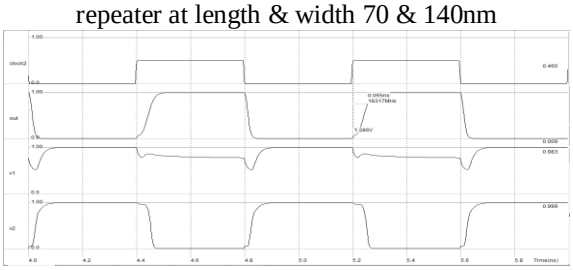

Fig. 8: Voltage vs Time waveforms of Boostable repeater at length & width 70 & 140nm

The Fig 8 shows the voltage versus time waveforms of Boostable repeater at length & width of 70 & 140nm. Clock2 signal is input and out is output of Boostable repeater. The conventional repeater repeats the voltage at input end. Here we get the output S3 is approximately equal to the input signal. The C_{pump} capacitor difference voltage will be the same

, The value v2 increases above V_{DD} this is increased up to 1v. This can be visualized as both v1 and v2 reach 1V with the time of 0.4 ns

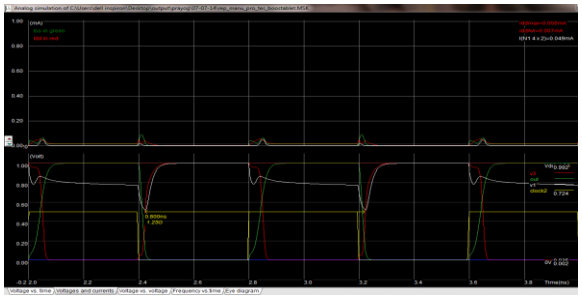

Fig. 9: Voltage vs Current waveforms of Boostable repeater at length & width 70 & 140nm

The Fig 9 shows the voltage versus current waveforms of Boostable repeater at length & width of 70 & 140nm.

A. Application Circuit Results

Here a chain of D-flip flops is taken as application circuit and conventional repeater and boostable repeater circuits are inserted and the results of those circuits are shown bellow.

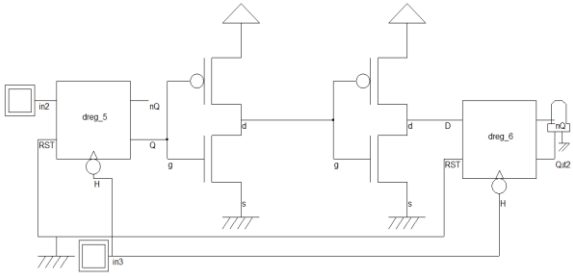

Fig. 10Transistor level diagram of chain of D-flip flops with conventional repeaters.

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue xx, Xxxxx 2014

The Fig 10 shows the transistor level diagram of chain of D-flip flops with conventional repeater. Here two negative edge triggered D-flip flops are taken as chain and in between those two conventional repeaters are inserted. And when the clock signal (in3) is low then only the output is raised equal to the input voltage (in2). The output voltage at the second bistable Multivibrator is approximately equal to the input voltage at the first Bistable Multivibrator.

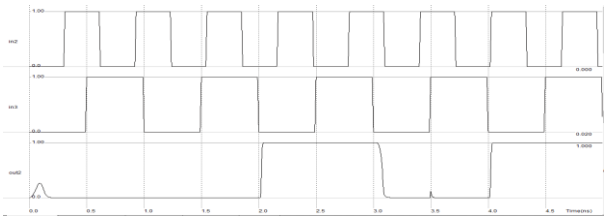

Fig. 11: Voltage vs Time waveforms of Chain of D-flip flops circuit with conventional repeater at length & width 70 & 140nm

The Fig 11 shows the voltage versus time waveforms of Chain of D-flip flops circuit with conventional repeater at length & width of 70 & 140nm. Here in2 is input signal and
in 3 used is the bistable multivibrator or D Flip Flop. Therefore it can be said that the voltage across the output and input is approximately equal. The D-flip flop is negative edge triggered, so the output is triggered whenever the clock signal (in3) is negative and we get the output approximately equal to the input voltage. But when conventional repeater is used some glitches are present in the output voltage which is shown in Fig 5.6.

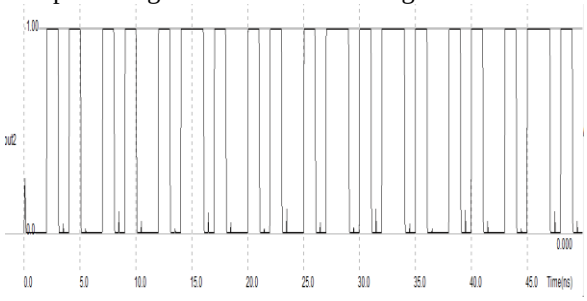

Fig. 12: Glitches in the output of Chain of D-flip flop circuit with conventional repeater.

The Fig 12 shows the glitches present in output of chain of D-flip flop circuit with conventional repeater, which are overcome by using Boostable repeater in the place of conventional repeater.

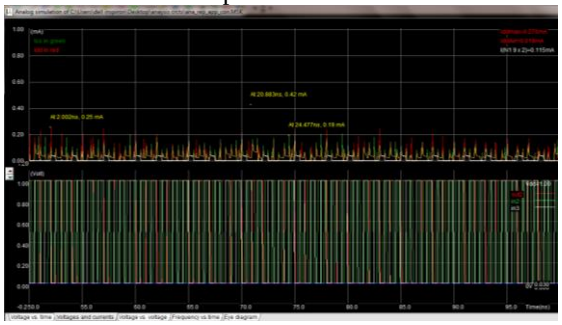

Fig. 13: Voltage vs Current waveforms of Chain of D-flip flops with conventional repeater at length & width 70 & 140nm

The Fig 13 shows the voltage versus current waveforms of chain of D-flip flops with conventional repeater at length and width of 70 & 140nm.

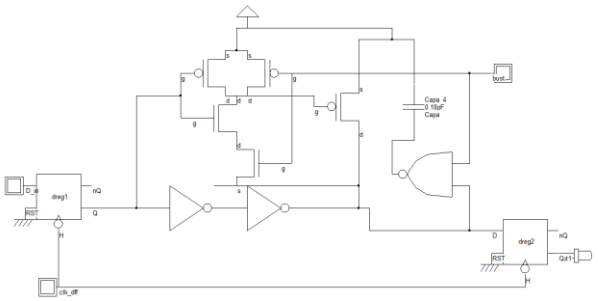

Fig. 14: Transistor level diagram of chain of D-flip flops with Conventional & Boostable repeaters.

The Fig 14 shows the transistor level diagram of chain of D-flip flops with Boostable repeater. Here two negative edge triggered D-flip flops are taken as chain and in between those two conventional repeaters are inserted. And when the clock signal (clk_dff) is low then only the output is raised equal to the input voltage (D_in). Therefore the voltage present across the output of flip flop is near by equal to the input voltage of that flip flop.

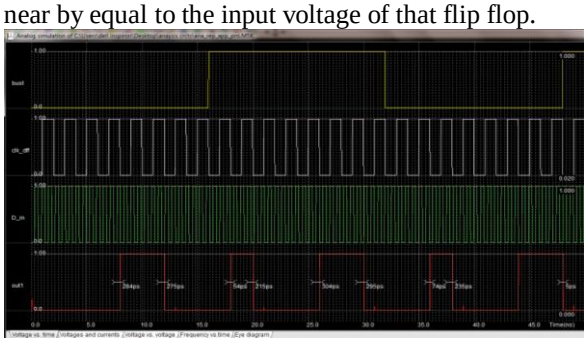

Fig. 15: Voltage vs Time waveforms of Chain of D-flip flops circuit with Boostable repeater at length & width 70 & 140nm

The Fig 15 shows the voltage versus time waveforms of Chain of D-flip flops circuit with Boostable repeater at length & width of 70 & 140nm. Here in2 is input signal and in3 is clock of D-flip flop,. The D-flip flop is negative edge triggered, so the output is triggered whenever the clock signal (in3) is negative and we get the output approximately equal to the input voltage. And Fig 6.14 shows the glitches in the D-flip flop circuit chain with Boostable repeater.

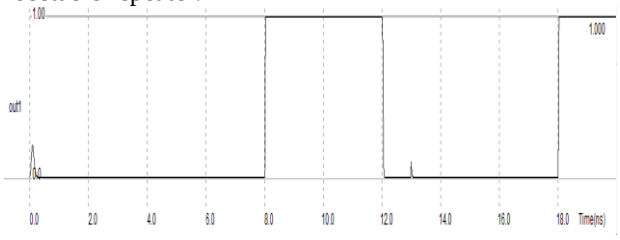

Fig. 16: Glitches in the output of D-flip flop chain circuit with Boostable repeater

Fig 16 shows the glitches in the output of D-flip flop chain circuit with Boostable repeater. When compared to the conventional repeater glitches are reduced when boostable repeater is used in the palce of conventional repeater.

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue xx, Xxxxx 2014

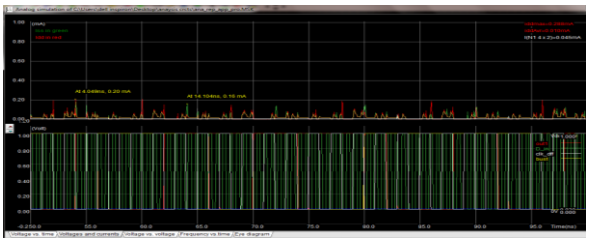

Fig 17: Voltage vs Current waveforms of Chain of D-flip flops with Boostable repeater at length & width 70 & 140nm

The Fig 17 shows the voltage versus current waveforms of chain of D-flip flops with Boostable repeater at length and width of 70 & 140nm.

VI.COMPARISON RESULTS

The experimental analysis gives a proof to the work carried these results are statistical values determining their length and width variations for conventional repeater and boostable repeater. The values given provide justification for various simulation works carried with power and delay variations. These elements decide the speed and switching action of the repeaters.

Rise time comparison between convention and boostable repeaters:

Table 6.1: Rise time comparison between conventional & boostable repeaters

	Rise time (ns)	
	Conventional Repeater	Conventional & Boostable Repeater
Individual repeater circuits	0.182	0.055
With chain of D-FF circuit	0.728	0.318
Chain of repeaters with D- FF circuit	1.046	0.929

From the above table, the rise time is less when boostable repeater is used along with the conventional repeaters. So, the switching speed is increased when boostable repeaters used.Power comparison between Boostable repeater & online adjustable buffer OAB:

Table 6.2: Power comparison between proposed repeater & OAB

Boostable Repeater	OAB
4.415 uw	15 – 18 uw

From the above table, the power dissipation is less when boostable repeater used than previous techniques OAB, ASV.

VII. CONCLUSION, FUTURE WORK & APPLICATIONS

The boostable repeater proposed has a novel method for improving the switching speed transiently at a sharp gap. This work has a new way of avoiding aging resilience and providing better voltage variations in an efficient manner. The work is compared with other D-Flip flop circuits and found appreciable results . Still there can be more improvements by reducing the charge pump leakage which helps in boosting the device more. More standardized approaches can be used for dynamic power management and automation Design.

A. Future Scope

The work can be still be improved by reducing the leakage power through capacitor and can be used in further circuits of online programming for parallel power management. Various factors may affect the performance measures of the designed boostable repeater such as termperature and variation in delay circuits. But still there is need of accurate result in performance measures.

B.Applications

1. Used in design, Fabrication of the systems
2. Much employed in leakage power design circuits

Interconnection of more number of complex circuits can be involved.

ACKNOWLEDGMENT

This work was supported by Rajeev Gandhi Memorial College of Engineering & Technology, Nandyal and special thanks to my guide for providing me enough support in completing this work.

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