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FPGA Implementation of Image Denoising using Adaptive Wavelet Thresholding

Ms. Chipy Ashok [1], Ms. Anu V.S [2]

M.Tech Student, ECE Department, SBCE, Pattoor, Kerala [1]

Assistant Professor, ECE Department, SBCE, Pattoor, Kerala [2]

Abstract: Visual information transmitted in the form of digital images is becoming a major method of communication in the modern age. But the main drawback in digital images is the inheritance of noise while their acquisition or transmission. Several noise removal algorithms have been proposed till date. One of the most powerful and perspective approaches in this area is image denoising using discrete wavelet transform (DWT). As the number of levels increased, Peak Signal to Noise Ratio (PSNR) of the image gets decreased, whereas and Mean Square Error (MSE) gets increased. The NeighShrink, BayesShrink, and VisuShrink are important methods to remove the noise from a corrupted image. These methods, however cannot recover the original image significantly since the threshold value does not minimize the noisy wavelet coefficients across scales and thus they do not give good quality of image. The adaptive denoising provides an adaptive way of setting up minimum threshold by shrinking the wavelet coefficients. This method retains the original image information efficiently by removing noise and it has the image quality parameters such as peak-to-signal noise ratio (PSNR). This thesis proposes a hardware implementation of adaptive thresholding algorithm using FPGA, which can reduce processing time considerably. The decomposition algorithm of discrete wavelet transform s designed and planned to simulate with the Hardware Description Language VHDL.

Keywords : Image denoising, discrete wavelet transform, adaptive thresholding, FPGA.

I. INTRODUCTION

The denoising of an image is a challenging task in the field of image processing. Image denoising is an important image processing task, both as a process itself, and as a component in other processes. There are many ways to denoise an image or a set of data exists. The NeighShrink, BayesShrink, and VisuShrink are important methods to remove the noise from a corrupted image. Recently, researchers have studied the dependency between wavelet coefficients and shrinking them has been shown to be a useful technique for image denoising especially for additive white noise. The wavelet denoising scheme thresholds the wavelet coefficients arising from the standard Discrete Wavelet Transform (DWT). Denoising of the natural image corrupted by Gaussian noise using wavelet techniques are very effective because of its ability to capture the energy of a signal in few energy transform values. The main advantages of the discrete wavelet transform over conventional transforms, such as the Fourier transform, are well recognized. Because of its excellent locality in time and frequency domain, wavelet transform is extensively and remarkable used for image processing like compression and denoising. DWT makes the energy of signal concentrate in a small number of coefficients hence the DWT of a noisy image consist of large number of coefficients with low signal to noise ratio (SNR), Removing this low SNR by selecting proper thresholding value. The denoising algorithm using DWT mainly has three steps, they are Forward Discrete Wavelet Transform (FDWT), Adaptive Thresholding and finally Inverse DWT (IDWT).

Here we are introducing a new method for thresholding which is the adaptive wavelet thresholding that shrinks the noisy coefficients. In this approach, the image is decomposed into subbands and the noisy coefficients are suppressed using hard and soft thresholding. The soft and hard thresholding involve forcing to zero the coefficients with amplitude lower than the selected threshold, and preserving (in hard) or shrinking (in soft) the coefficients greater in this threshold with the threshold value.

The 2-D DWT has been widely applied for medical applications as it provides perfect reconstruction property. However, it involves several computational steps to calculate DWT coefficients. The decomposition and reconstruction computation of the DWT is computationally intensive process especially for 2-D and may fall short in meeting real-time applications. So, efficient hardware design of DWT is required to achieve the desired goals.

The performance of the implementation can be improved by exploiting the parallel processing platforms. Field Programmable Gate Arrays (FPGA) is a powerful hardware parallel processing platform that offers parallel and pipeline architecture, large hardware resource, flexibility, adaptability, and low cost. It also offers embedded processors and memory resources. This option offers versatility in running diverse software applications on embedded processors, while taking advantage of reconfigurable hardware resources, all on the same chip package. The only challenge of FPGA is the requiring of low level programming.

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II. DISCRETE WAVELET TRANSFORM

Mallat algorithm is proposed in 1988 as a fast algorithm of discrete wavelet transform. As a leading theory of DWT hardware realization, it is widely used in DWT, just as the fast Fourier transform used in the classical Fourier analysis.

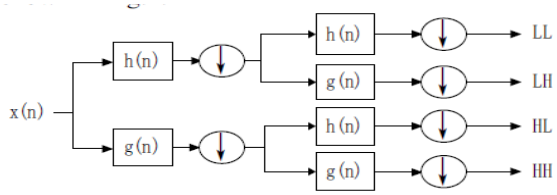

Fig.1. Schematic diagram of two-level DWT

Figure 1 gives a DWT structure based on Mallat algorithm. Using this method, DWT can be efficiently implemented by using cascaded quadrature mirror filters (QMFs), which are comprised of a high-pass FIR filter, a low-pass FIR filter and two 2-extraction stages, respectively. In the field of image processing, what the need to deal with are the two-dimensional data matrix. Therefore, the Mallet algorithm should be extended to the two-dimensional space. This is essentially to make twice one-dimensional wavelet transform to the image matrix. Firstly, the filter groups h (n) and g (n) are used for each row of the image to filter and 2 extract, and then each column of the results use the same filter to filter and 2 extract. In this way, the original image is decomposed into four sub-band images, denoted as LL, LH, HL and HH. Where the LL stands for the horizontal and vertical low signal; the LH for the horizontal direction's low pass and vertical direction's high-pass signal ;the HL for the horizontal direction's high pass and vertical direction's signal, and the HH is the horizontal and vertical direction high-pass signal. The sub-band LL represents the coarse-scale DWT coefficients while the sub-bands LH, HL and HH represent the fine-scale of DWT coefficients. To obtain the next coarser scale of wavelet coefficients, the sub-band LL is further processed until some final scale N is reached. This process is generally called as "Subband Decomposition"

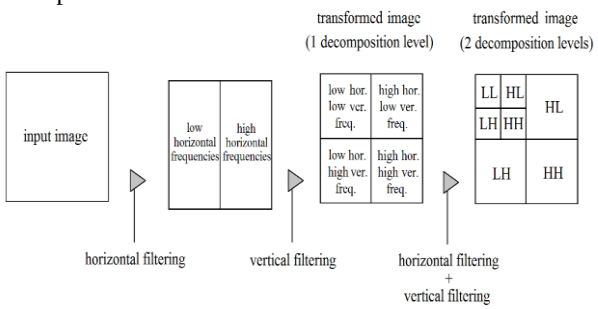

Fig. 2: Application of two levels of DWT decomposition to an image.

Figure 2 depicts this scheme when two levels of decomposition are applied to an image. The reverse DWT applies the inverse procedure starting at the last level of decomposition.

A. Haar Wavelet

Here haar wavelet is used for the process of image denoising It is the oldest and simplest orthonormal wavelet which is prominent in terms of memory consumption and despite other wavelets without any influence of edge, is completely recursive. Haar wavelet does not possess overlap windows and only reflects the changes between two adjacent pixels. Also since it uses just two functions as scale and wavelet, it calculates average and difference of a pair. Each step in the forward haar transform calculates a set of wavelet coefficients and a set of averages. If a data set contains n elements, there are nl2 averages and nl2 coefficient values. Scaling and Wavelet functions for haar wavelet are given in (2) & (3) respectively. Where So to Sn_1 are image data, a is averaging, d is differencing.

$$a = {}^{(S_i + S_{i+1})}/_{2} \quad (1)$$

$$d = {}^{(S_i - S_{i+1})}/_{2} \quad (2)$$

Haar average is calculated by the scaling function and coefficient is calculated by the wavelet function. Haar wavelet operates first on adjacent horizontal elements and then on adjacent vertical elements. As each transform is computed the energy in the data in relocated to the top left hand comer. After each transformation the dimensions of resulted image cut into two halves. The transformation of 2D image is a 2D generalization of the ID wavelet transforms.

First, ID wavelet transform applied to each row of pixel values. This operation gives average value along with the detail coefficients for each row. Next these transformed rows
are treated as if they are themselves as an image and ID transform is again applied to each column. This process is repeated recursively only on quadrant containing averages. The image is comprised of pixel represented by numbers. Consider a image of 4 By 4. The matrix (2D array) representing an image is as shown below,

$$\begin{bmatrix} 5 & 4 & 3 & 6 \\ 5 & 4 & 3 & 6 \\ 6 & 3 & 8 & 9 \\ 3 & 2 & 7 & 6 \end{bmatrix}$$

The result of haar wavelet transformation on rows by performing averaging and differencing operation is as shown in following matrix.

$$\begin{bmatrix} 4.5 & 4.5 & 0.5 & -1.5 \\ 4.5 & 4.5 & 0.5 & -1.5 \\ 4.5 & 8.5 & 1.5 & -0.5 \\ 2.5 & 7.5 & 0.5 & 0.5 \end{bmatrix}$$

Again this above result is treated themselves as an image and again haar wavelet transformation is carried out on columns of matrix (image) by performing averaging and differencing operation .The result is given in last matrix and this is a result of haar wavelet transformation at first level.

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$$\begin{bmatrix} 4.5 & 4.5 & 0.5 & -1.5 \\ 3.5 & 8 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0.5 & 0.5 & -0.5 \end{bmatrix}$$

At second level, input will be only average component of the first level decomposed image. This process is repeated up
to three levels. Figure 3 and Figure 4 shows an lenna image after haar wavelet transformation applied at first level, second level, repectively.

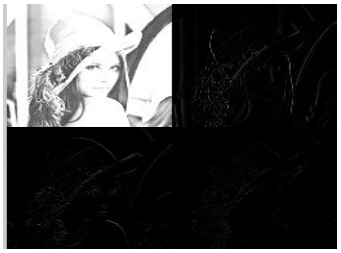

Fig.3: First level of decomposition of image lenna

Fig.4: Second level of decomposition of image lenna

III. ADAPTIVE WAVELET THRESHOLDING

Suppose that a given original image, S, has been corrupted by additive Gaussian White noise, Z, with independent identical distribution (i.i.d) i.e *M (0, σ^2)*. The corrupted image X is defined as

$$X = S + Z \quad (3)$$

Our goal is to denoise the noisy image *X* in order to estimate an image *S** , as close as possible to original image *S* in the sense of the mean squared error (MSE). There are various methods for threshold evaluation that shrink the noisy coefficients. The VisuShrink uses the threshold function, denoted by *T1*, that is proportional to the standard deviation of the noise [6]. This threshold is also referred as univeral threshold and is given as

$$T1 = \sigma\sqrt{2\log M} \quad (4)$$

Where σ^2 represents the noise variance which is defined based on the median absolute deviation as follows

$$\sigma^2 = [\frac{median[X\,(m,n)]}{0.6745}]^2 \quad (5)$$

Here $X(m,n) \in HH1$

The VisuShrink method however yields an overly smoothened image since the threshold estimation is derived under the constraint with high probability.

The modified threshold, denoted by T2, overcomes this shortcoming [12]. which is given as

$$T2 = \sigma\sqrt{2\log M*} \quad (6)$$

Where $M* = \frac{M}{2^k}$, an image dimension at k^{th} decomposition level.

The NeighShrink incorporates neighbouring coefficients in thresholding estimation. This method groups the wavelet coefficients in non-overlapping blocks and then thresholds them empirically blockwise. Let $Sq\ m,n^2$ be the summation of square of wavelet coefficients, denoted by *dp,q* We have

$$Sq\ m,n^2 = \sum_{k=0}^{n} dp,q^2 \quad (7)$$

These methods, however , are not able to remove noise efficiently as they remove many coefficients because of absolute large threshold value , Therefore, we try to overcome this shortcoming by modifying all the detailed noisy coefficients using exponential function which leads to the exponential decay of the wavelet coefficients across scales. Therefore, a new adaptive threshold , *Tn* is defined below that removes the noise efficiently.

A. Estimation of Threshold

The new threshold, *Tn, is defined as follows*

$$Tn = f(t)\sigma\sqrt{2\log M* - k} \quad (8)$$

Here f(t) is an improving factor, defined as

$f(t) = e^{\frac{-t}{t+1}}$, t > 0, an integer

B. Algorithm

The steps of the proposed algorithm are given as [1], [2]:
Input: noising image i.e. corrupted with Gaussian noise
Output: denoised estimate of original image
Begin

i. Perform 2-D DWT on noisy image up to kth decomposition level.
ii. For each decomposition level of the details subband i.e. *HH, HL,*, and *LH* with the wavelet coefficients do
Calculate the new threshold, *Tn* using (6)
Apply the shrinkage factor to obtain the noiseless wavelet coefficients
End{do}
iii. Repeat steps (i) and (ii) for all decomposition levels.
iv. Reconstruct the denoised estimate image

IV. FPGA IMPLEMENTATION

The field-programmable gate array (FPGA) is a type of programmable device. Programmable devices are a class of general-purpose chips that can be configured for a wide variety of applications, having capability of implementing the logic of hundreds or thousands of discrete devices. Programmable read-only memory (PROM), erasable programmable read-only memory

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(EPROM) and electrically erasable PROM (EEPROM) are the oldest members of that class, while programmable logic device (PLD) and programmable logic array (PLA) represent more recent attempts to provide the end-user with an on-site customization using programming hardware. This technology, however, is limited by the power consumption and time delay typical of these devices. In order to address these problems and achieve a greater gate density, metal programmed gate arrays (MPGA) were introduced to programmable logic industry market. An MPGA consists of a base of pre-designed transistors with customized wiring for each design. The wiring is built during the manufacturing process, so each design requires expensive custom masks and long turnaround time. Since FPGAs are application-specific ICs it is often argued that FPGA is an application specific integrated circuit (ASIC) technology.

FPGAs offer the benefits of both PLD and MPGA. In fact, the computing core of an FPGA consists, in general, of a highly complex re-programmable matrix of logic IC, registers, RAM and routing resources. These resources can be used for performing logical and arithmetical operations, for variable storage and to transfer data between different parts of the system. Furthermore, since there is no centralized control and sequential instructions to process, typically thousands of operations can be performed in parallel on an FPGA during every clock cycle. Though the clock speed of FPGAs (20-130MHz) is lower than of current RISC systems (100-500MHz), the resulting performances are comparable in many applications such as image and video processing and data encryption. The SRAM FPGA gets its name from the fact that programmable connections are made using pass-transistors, transmission gates, or multiplexers that are controlled by static random access memory (SRAM) cells. The advantage of this technology resides in the fact that it allows fast in-circuit reconfiguration. The major disadvantage, however, is the size of the chip required by the SRAM technology.

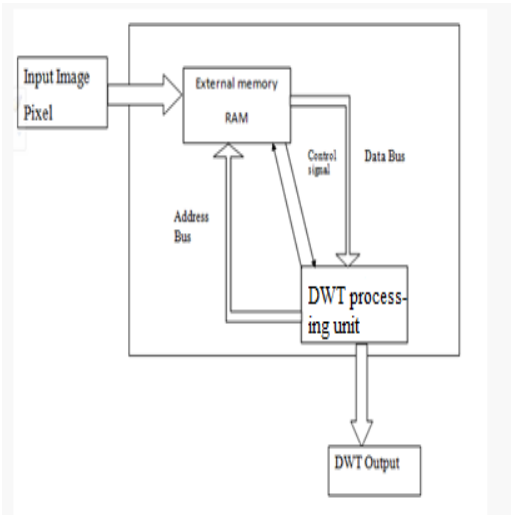

Fig. 5: Forward DWT Architecture

Architecture, continuing with the analogy of an IC, is equivalent to the internal electronic circuit that performs the function for which the component has been designed. At this stage all the signals the entity uses to communicate with the external world are defined and unchangeable. Inside the entity, instead, the programmer can write any type of statements allowed by the VHDL syntax, like other components, representing subcircuits, other signals, to connect them, or processes, which contain sequential statements operating on values. The purpose is only that to apply some operations to data on input ports and generate some results to assign to output ports. Within architecture the programmer can concentrate on the descriptive part of the system, but the divide and conquer motto can be applied once again. VHDL, indeed, offers the opportunity to choose the desired abstraction level. Thus, for a first behavioral version, aiming to investigate a circuit feasibility or correctness, code lines containing high level data types or cumbersome mathematical formulas and few electronic details will be advisable. Then, a subsequent description can go further and optimize the implementation with clever solutions for better performance, smaller area and fulfillment of constraints.

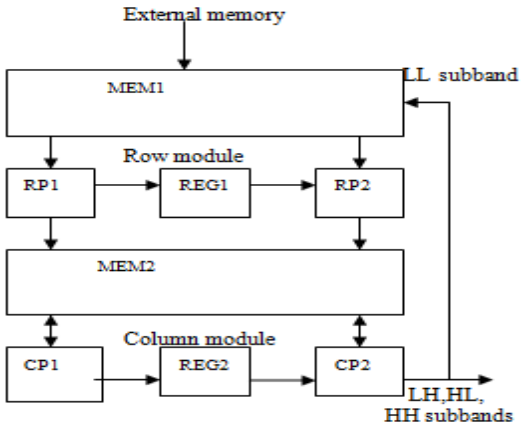

Fig. 6: DWT processing unit.

The architecture can compute a large set of filters for both the 2D forward and inverse transforms. It supports two classes of architectures based on whether lifting is implemented by one or two lifting steps. The one step architecture corresponds to implementation using one lifting step or two factorization matrices.

A. XESS XSV Virtex FPGA Board

The XESS XSV board contains a CPLD and a XCV800 FPGA with 800,000 gates. It has the capability of processing audio and video signals. It can output these video signals through its 110MHz, 24-bit RAMDAC. It also contains two independent RAM banks of 512K x 16 SRAM used for local buffering of data and signals. The XSV800 Board has a variety of interfaces: serial and parallel ports, Xchecker cable, USB port, PS/2 keyboard and mouse ports, and 10/100 Ethernet PHY layer interface. There are also two independent expansion ports.

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The Virtex FPGA is a programmable logic device that transmits/receives address and data signals to and from the two independent SRAM banks. It also conveys control information to the both SRAM banks using the clock. The FPGA can also generate a video signal that can be displayed on a VGA monitor using a BT481A RAMDAC.

SRAM: The FPGA has access to two independent banks of SRAM. Each SRAM bank is organized as 512K × 16 bits. Each bank is made from two Alliance AS7C4096 memory chips of organization 524,288 words x 8 bits. Each of the 4 SRAM chips is directly connected to the FPGA . Two each of them form the left memory bank and the right memory banks, giving 1MB RAM each for the left bank and the right bank. The embedded memory is accessible for read/write from both the computer (through the XSV SRAM Utility) as well as from the FPGA. Each of the 1MB memory bank is organized as 524288 words of 16 bits each. The image data is stored in the left SRAM bank. The FPGA reads and process the image and writes the result to the right SRAM bank.

V. EXPERIMENTAL RESULTS

TABLE 1: PSNR COMPARISON CHART OF OUR PROPOSED METHOD WITH OTHER STATE OF ART METHODS

Image	PSNR Values for various denoising methods		
Lenna	Noise levels	Mantosh Biswas et al; (t=2)	Proposed method (t=2)
	10	34.25	34,874
	20	30.08	30.704
	30	27.56	28.184
	50	24.8	25.424
	100	22.43	23.054

VI. CONCLUSION

The wavelet denoising techniques offer better quality and some flexibility for noise problems of signals and images. In this work, the proposed 2D-DWT architecture for image denoising using a an adaptive thresholding which introducing a exponential decay of noisy wavelet coefficients, this method proves fast and easy hardware implementation, few and simple arithmetic computations, and occupies less memory storage, therefore it is appropriate for FPGA solutions. An optimized FPGA implementation of DWT method is developed which includes all its dimensions. It provides high throughput rate compared with other implementations with slightly increasing in the number of occupied slices and power dissipation.

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