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Low Power Double Gate Fin FET Based Sense Amplifier

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Abstract*:* In this paper, a low power independent-gate, process variation tolerant double gate (DG) Fin FET based sense amplifier design has been proposed. As like RHIGSA, new design exploits the DICE (dual interlock cell) latch and the back gate of a double-gate Fin FET (DG Fin FET) device for dynamic compensation against process variation. But, there is change in tail transistor gate connections.,Which is dynamically controlled by intermediate signal in circuit. This design improves the power dissipation and show excellent tolerance to process parameter variations like temperature, V_{dd}, thickness of oxide compared to Radiation hardend IGSA (RHIGSA) circuit and independent gate sense amplifier (IGSA). Proposed technique consumes 29.108% less power compare to RHIGSA.

Keywords*:* Double Gate FIN FET, Sense Delay, Process Variation, Montecarlo Simulation

1. INTRODUCTION

Performance of embedded memory and its peripheral circuits like sense amplifier, write driver, row decoder and column decoder can adversely affect the speed and power of overall system. Sense Amplifier is the most vital circuits in the periphery of CMOS memory as its function is to sense stored data from read selected memory. Whenever, a small difference bit line is sensed(less than 50mV). The performance of sense amplifiers strongly affects both memory read access time, operating speed of memory and overall memory power dissipation. The latch-based sense amplifiers are designed to be symmetric but with the process variations it becomes asymmetric. If the difference in voltage at bit-lines, formed due to process variations, is sufficient to overcome bit differential voltage developed, then the sense amplifier may latch incorrect signal. This will affect the overall functionality of the circuit. Functional yield is defined as the ratio of number of correct sensing operations to the total number of sensing operations. A typical memory chip may contain a large number of sense amplifiers and if some sense amplifiers malfunction then it causes loss of functional yield. Hence it is necessary to design robust sense amplifiers that have lower failure probability against process variations. The primary design concerns in sense amplifier are sensing delay, power consumption and tolerance to mismatch and process variations [1–4]. The performance of sense amplifiers is determined primarily by the sensing delay. It is necessary to reduce the sensing delay to have a high performance sense amplifier. The robustness of the sense amplifier is determined by the input offset voltage i.e. the minimum voltage difference(less than 50mV) between the bit-lines that can be correctly sensed.

The multi gate Fin FET technology [5] is a latest substitute, among the existing FET to conventional single gate technologies. Double-gate devices can be designed in different ways, namely: (1) symmetrical device (2) asymmetrical device. Based on the gate connection, double-gate Fin FET's can be classified as tied gate and independently controlled gates. Choice of these configurations gives more flexibility to the designer to selectively control the devices. Recently, the benefit of using independent gate control in double gate devices for efficient circuit design is already demonstrated [6,7]. It is also reported that the intrinsic fluctuations in double gate architectures will reach levels that will affect the yield of the next generation circuits unless appropriate changes to the design are made [8].

The Fin FET transistor is a vertical double gate device and is regarded as a promising alternative for sub-45 nm bulk devices [9]

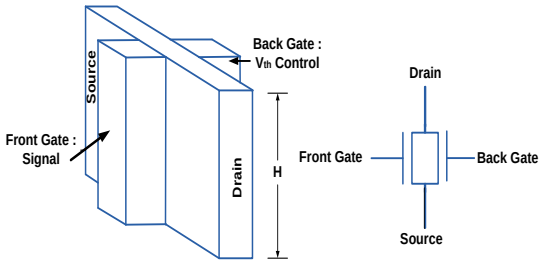

Fig.1. Double Gate Fin FET Structure and Symbol

Figure 1 shows the structure of a double-gate Fin-FET device. Current flow is parallel to the wafer plane. The thickness t_{si} of the single fin is equal to the silicon channel thickness. Each fin contributes to the width of the device, and H is the height of each fin. The Fin FET circuit behavior can be studied using PTM (Predictive Technology Model) of 32 nm CMOS Fin FET technologies [10].

A unique property of the Fin FET is the electrical coupling between the front and back gates. The implication of this coupling is that the threshold voltage of the front gate (V_{thf}) is not only established by the process, but also it can be controlled by the back gate voltage (V_{Gb}). This is similar to the body effect in a bulk transistor.

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An independent gate Fin FET operates in the dual gate mode (DGM) when both gates are biased to induce channel inversion. Alternatively, an independent gate n-Fin FET (p-Fin FET) operates in the single gate mode when one of the gates is deactivated by connecting the gate to ground (V_{DD}). Disabling one of the gates in the single gate mode (SGM) increases the absolute value of the threshold voltage compared to DGM. Therefore, it is possible to modulate the threshold voltage of the Fin FET by biasing the two gates independently [11].

We have used the following device parameters [12] in our work: effective channel length of Fin FET (L_{eff}) = 32 nm, (T_{fin}) = 8 nm, height of silicon fin (H_{fin}) = 32 nm, geometrical channel width (W_{fin}) = ($2H_{fin}$) + T_{fin}, front gate oxide thickness (t_{fox}) = 1.4 nm, back gate oxide thickness (t_{box}) = 1.4nm, V_{dd}= 0.8V, V_{th} of NMOS = 0.25 V and V_{th} of PMOS = -0.25 V.

In particular, this paper makes the following contributions:
(1) Modified radiation hardened sense amplifier based on double gate Fin FET technology is presented, which consume less power than existing(RHIGSA).
(2) Tolerance to process parameter variation like Voltage, Temperature and Thickness of oxide.

2. DEVICE DESIGN

2.1 Working Methodology

- This chart shows the design strategies for SRAM sense amplifier circuit.
- As continuous scale down in FET technologies will increase the chance of design mismatch. So process variation is very important.
- We will apply this design flow on latch based sense amplifier like IGSA \ RHIGSA using FINFET.

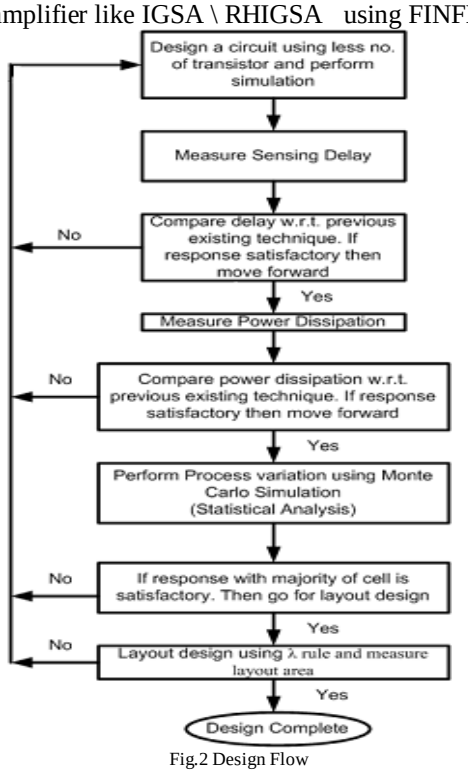

Fig.2 Design Flow

2.2. The Proposed Sense Amplifier

The frequently used latch type sense amplifiers are classified as two types: (1) current latch sense amplifiers [13] and (2) voltage latch sense amplifier [14]. Sense amplifiers are designed for lower sensing delay and smaller input offset voltage [15]. Voltage latch sense amplifiers cannot reliably sense small signals, develops output signals slowly and severely limits radiation hardness in scaled devices [16]. The current latch sense amplifier called independent gate sense amplifier (IGSA) as shown in Fig.3 is reported by Mukhopadhyay et al. [7]. And another current latch sense amplifier called radiation hardened independent gate sense amplifier (RHIGSA) as shown in Fig.4 is reported by Rathod et al.[17].

The radiation hardened independent gate sense amplifier (RHIGSA) based on DICE (Dual Interlock Cell) latch. Since DICE latch [18] is used in the design, RHIGSA name has been adopted. DICE latch is widely used to achieve the immunity against single event upset (SEU). It consists of a symmetrical structure of four CMOS inverters as shown in Fig.3. Each inverter has NMOS and PMOS separately controlled by two adjacent nodes storing the same state. The four adjacent nodes of the DICE cell form a pair of latches in two alternate ways, depending on the stored logic value. One of the adjacent nodes controls the conduction state of the transistor connecting the current node to a power supply, and the other node blocks the complementary transistor of the inverter, isolating it from the opposite supply line. The two adjacent nodes are logically isolated and must be reverted in order to upset the latch. In the DICE latch, the node that is affected by SEU or by the variation in process parameters is driven back to its previous state by other transistors. We combined the benefit of DICE latch and independently controlled technology, for improving radiation hardness and speed to achieve the radiation tolerant fast sense amplifier.

The operation of sense amplifier has two phases namely pre-charge and sense signal amplification. In the pre-charging phase, sense enable (SEN) signal is kept 'low' (Fig. 5) and the output nodes Out1 (i.e. O3) and Out2 (i.e. O4) are pre-charged to V_{dd} by the two pre-charging transistors X10 and X11 (Fig. 5). Bit-lines are used to transfer data between sense amplifier and static random access memory (SRAM). Bit-lines are charged to $V_{dd}/2$. Bit-line and bit line- bar signals are represented by 'bl' and 'blb' respectively. Signal 'blb' is chosen as linearly decreasing dc voltage from $V_{dd}/2$. In the sensing phase, SEN signal goes 'high'. This activates the cross coupled structure and drives the outputs to the appropriate values. A stronger current is developed in transistor X5 than transistor X6 due to the higher gate input voltage, thus node 'O1' discharges faster than node 'O2'. The rapid drop of node voltage 'O1' turns 'on' the transistor X2, thus charges node 'O2' back to V_{dd}. With node 'O1' continuing to discharge, a full swing signal is obtained between the output nodes 'O3' (Out1) and 'O4' (Out2) resulting in a correct sensing operation.

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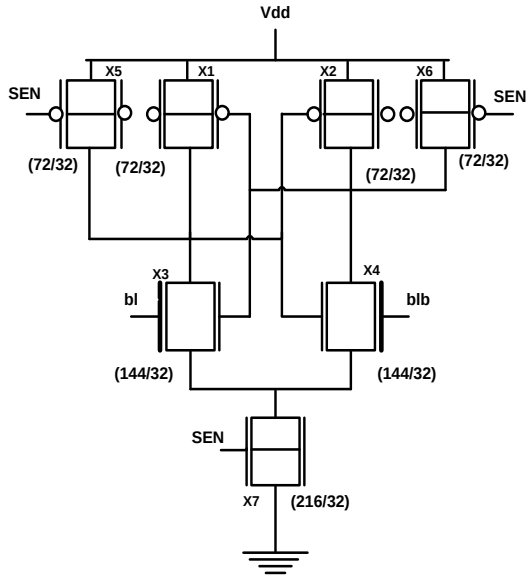

Fig. 3 Independent-gate sense amplifier (IGSA) circuit. [7]

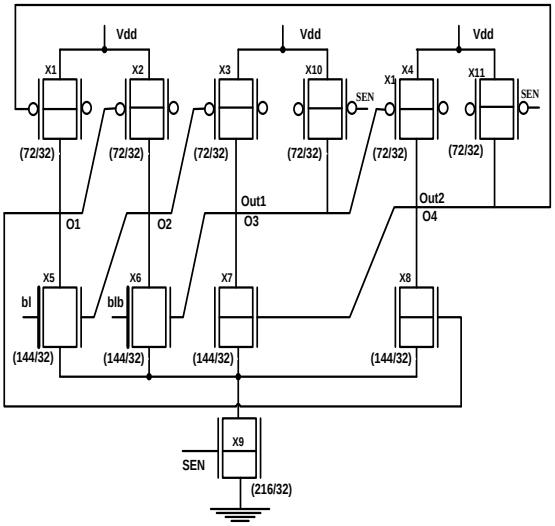

Fig.4 Radiation hardened IGSA (RHIGSA) circuit. [17]

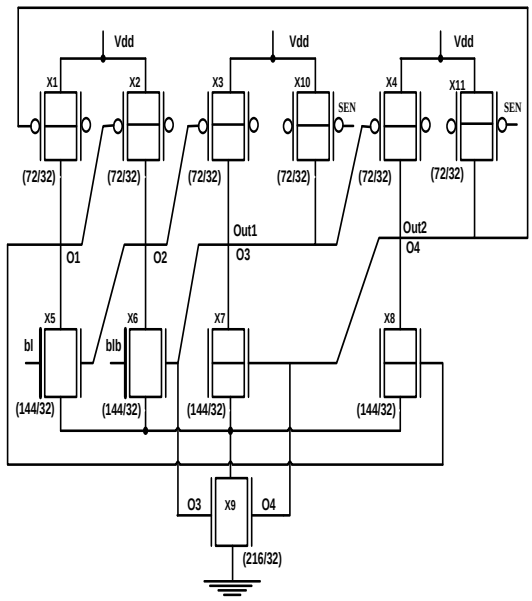

Fig.5 Proposed Low Power radiation hardened IGSA (LPRHIGSA) circuit

In the RHIGSA design, critical transistors X5 and X6 that are most sensitive to process variations are independently controlled, while rest of all the transistors have tied gates. Front gates of transistorsX5 and X6 are connected in cross-coupled inverter configuration whereas 'bl' and 'blb' are connected to the back gates. Under this situation, similar to IGSA, threshold voltage of transistors X5and X6 are dynamically controlled by the bit-lines. It is interesting to note that RHIGSA has separate input and output nodes. Hence, RHIGSA has accelerated sensing speed, and it can be used for low voltage operation.

All the PMOS transistors are minimum sized to reduce the area requirement. To reduce the probability of failure, NMOS transistors are upsized. The upsizing of NMOS transistors lower the trip point voltage that flips the cross-coupled inverters at a lower output voltage. Transistor X9 is connected to all the paths of cross-coupled inverters; hence it is widely sized (three times the minimum-sized transistor) however its variation will affect all the paths equally. The 'high' logic level of IGSA does not reach full V_{dd} value and hence logic swings for these types of amplifiers are reduced.

Proposed low power radiation-hardened independent-gate sense amplifier Sense amplifier (LPRHIGSA) based on RHIGSA in which tail transistor X9 is controlled by node O3 and O4 as shown in Fig.4. This method can decrease the threshold voltage of transistor X9 at the start of sense operation; otherwise increase the threshold voltage of transistor X9 at the end of sense operation. Resulting power dissipation reduced up to 29%.

3. RESULTS AND DISCUSSION

To examine the reliability of Integrated circuit, it is necessary to study the impact of process variations by statistical methods [19]. We have performed Monte Carlo analysis for 1000 iterations with 3σ parameter variations to estimate the tolerance with sense delay with 10% variation in Length and Width of Fin FET.

HSPICE [20] simulations have been carried out with the 32-nm Berkeley 'Predictive Technology Model' for double gate Fin FET device [12]. For a 64 KB of memory we have 512 cells connected to each bit-line, resulting in an equivalent capacitive load of about 450 fF [21]. A typical value equal to 1pF for bit-line capacitance and value for a load capacitance of 370 fF are used. Supply voltage was maintained at 0.8 V for all types of sense amplifiers.

3.1 Impact of process variations

Impact of channel length (L_{fin}) mismatch and fin width (W_{fin}) mismatch on sense delay of sense amplifiers is studied in this section. Failure probability of current latch sense amplifiers is more than voltage latch sense amplifiers because they are susceptible to both current mismatch and trip point mismatch. In this work, we have presented simulation results for the current latch sense amplifiers.

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Fig.6 shows the effect of process variation on IGSA, RHIGSA and LPRHIGSA for Wfin and Lfin distribution (3σ) obtained by Monte Carlo simulation of 1000samples. It can be observed that out of 1000 samples RHIGSA and LPRHIGSA shows less variation in sense delay than IGSA.

3.2 Sense Delay

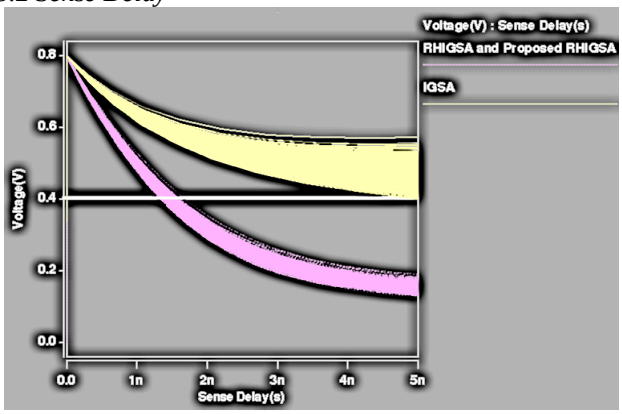

Fig.6 Circuit characteristics for Wf_{in} and L_{fin} distribution (3σ) obtained by Monte Carlo (1000 iterations) for IGSA, RHIGSA and LPRHIGSA

Sense delay is one of the important parameter that decides performance of a sense amplifier. Sense delay is defined [22] as time at which sense enable signal rises to $V_{dd}/2$ to the time at which output drops to $V_{dd}/2$.

A decrease in number of transistors in the stack increases the gain of the cross-coupled inverters, increases the discharging current, and increases the difference in the current produced by the

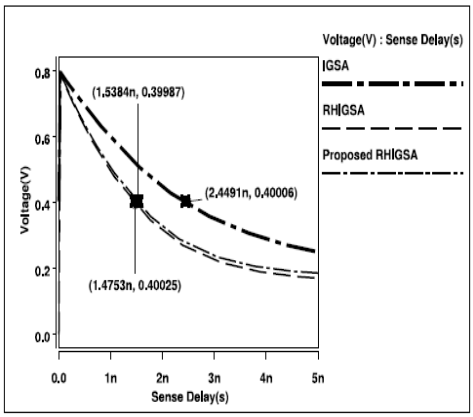

Fig. 7 Sense delay comparison

application of minimum voltage at the bit-lines. RHIGSA has only one stacked transistors in the critical path.

Also the additional pair of inverters in RHIGSA minimizes the impact of process variations on the critical transistors by restoring the state of the critical node. This property increases the tolerance to the noise and process variations.

Sense delay increases due to W_{fin}, L_{fin} and T_{ox}. Sense delay for IGSA is very large as compared to sense delay of RHIGSA and LPRHIGSA (Fig.7). Asymmetric devices with increased back gate bias are used for short circuit current reduction. This will reduce the short circuit power; however it increases the sense delay (Fig.8).

Sense delay is increased due to the decrease in the 'on' current. The 'on' current is reduced because of reduction in the discharging currents of Out1and Out2 nodes.

This is primarily because of reduced difference between the currents of X5 and X6 (Fig. 4) transistors produced due to differences in the back gate bias for asymmetric devices. FromTable-1 it should be noted that RHIGSA has less sense delay than IGSA.

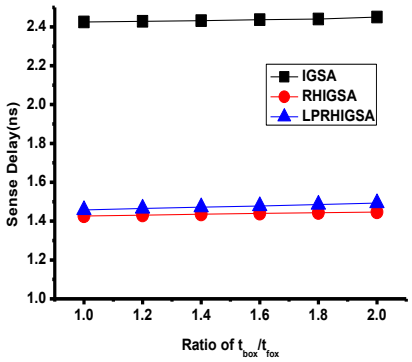

Fig.8 Sense delay against variation in back gate oxide thickness.

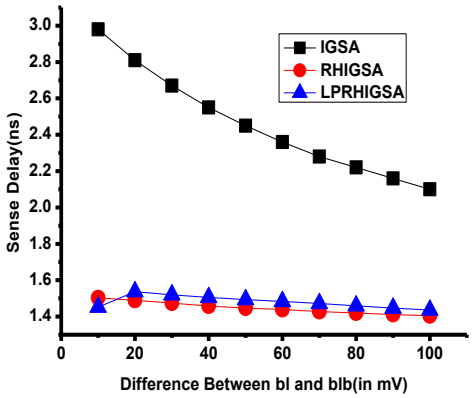

Fig.9 Sense delay against bit-line differential voltage.

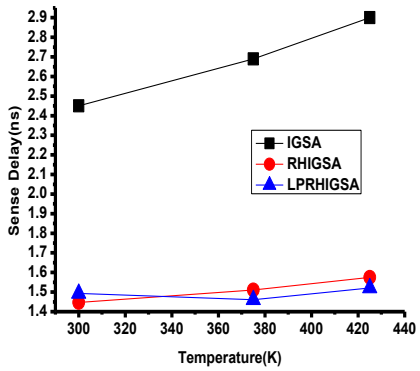

Fig.10 sense delay against different temperature In Kelvin.

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Vol. 4, Issue 3, March 2015

Table-1 Sense Delay for variation in back gate oxide thickness when V_{dd}=0.8V

Sense Delay For(in ns)	t_{box}/t_{fox} Ratio					
	1.0	**1.2**	**1.4**	**1.6**	**1.8**	**2.0**
IGSA	2.425	2.428	2.432	2.437	2.440	2.450
RHIGSA	1.426	1.431	1.436	1.440	1.443	1.447
LPRHIGSA	1.458	1.465	1.472	1.478	1.485	1.493

Table-2 Sense Delay for ΔV(mV) when VDD=0.8V and t_{box}/t_{fox} Ratio=2

Sense Delay For(in ns)	Difference between bit and bit bar, ΔV(mV)									
	10	20	30	40	50	60	70	80	90	100
IGSA	2.98	2.81	2.67	2.55	2.45	2.36	2.28	2.22	2.16	2.10
RHIGSA	1.503	1.489	1.474	1.458	1.447	1.439	1.427	1.419	1.411	1.404
LPRHIGSA	1.452	1.537	1.519	1.505	1.493	1.483	1.472	1.459	1.447	1.436

Table-3 Sense Delay for temperature when V_{DD}=0.8V and t_{box}/t_{fox} Ratio=2

Sense Delay For(in ns)	Temperature Variation(in Kelvin)		
	300	375	425
IGSA	2.45	2.69	2.90
RHIGSA	1.447	1.511	1.575
LPRHIGSA	1.493	1.461	1.521

Temperature variation may cause performance degradation, which may lead to functional failures [23]. Sense delay is obtained for change in bit differential voltage and increase in temperature as shown in Figs (table2-3) respectively. However it decreases with the increase in the offset (bit-line differential voltage).

3.3 Layout Area

Layout for IGSA is as shown in Fig. 11. The extracted value of parasitic capacitances at node 'Out1' and 'Out2' for IGSA (Fig.3) are 3.01fF and 3.01fF respectively. Layout for RHIGSA is as shown in Fig. 12. For RHIGSA

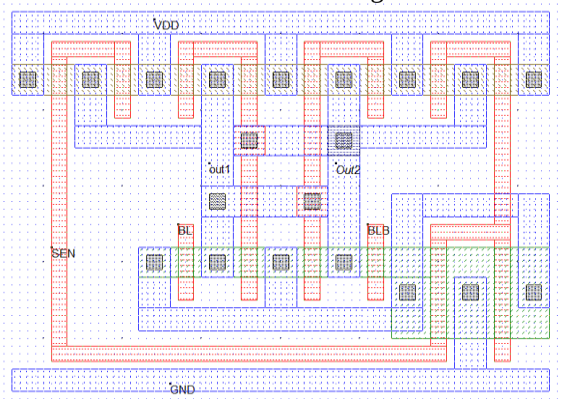

Fig.11Layout of IGSA

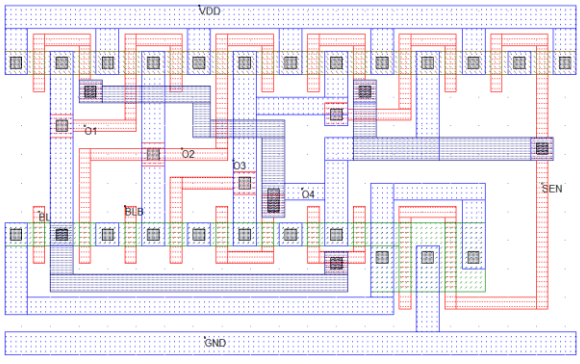

Fig.12 Layout of RHIGSA

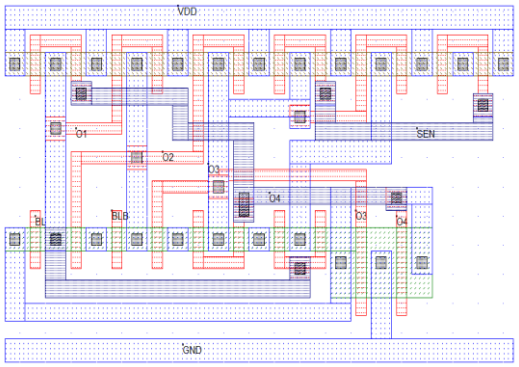

Fig.13Proposed Modified RHIGSA (LPRHIGSA)

(Fig. 4), the extracted parasitic capacitances at nodes 'Out1', 'Out2', 'Out3' and 'Out4' are 1.78fF, 1.24fF, 1.47fFand 1.96fF respectively. Similarly, Layout for LPRHIGSA is shown in Fig. 13. , The extracted parasitic capacitances at nodes 'Out1', 'Out2', 'Out3' and 'Out4' are 1.78 fF, 1.24 fF, 2.39 fF and 2.53 fF respectively. Capacitance for the layout is carefully designed so that sensitive pairs do not come in close proximity. This can help in increasing the critical charge thereby increasing the single event hardness. Due to the large number of transistors, LPRHIGSA and RHIGSA consume 75.75% more area as compared to IGSA. The merging of the PMOS pull up transistors X3, X4 and pre-charging transistorsX10, X11 can be done to reduce the area.

3.4 Power dissipation

Power dissipation for one complete read cycle of sense enable (SEN) signal is evaluated for all three type of sense amplifiers and results are presented in Fig.14 (table-4). It can be observed that short circuit current and hence average power dissipation can be reduced by increasing the asymmetry. Decrease in power dissipation by 17.21%, 14.83% and 19.66% for IGSA, RHIGSA and LPRHIGSA respectively has been observed after making the back gate oxide thickness double as compared to the front gate oxide thickness (t_{box}/t_{fox} = 2) for critical transistors.

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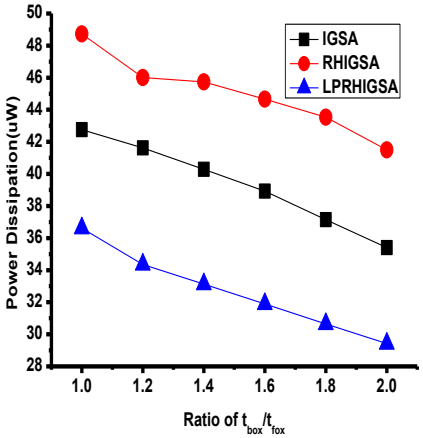

Fig.14 Power dissipation against variation in back gate oxide thickness.

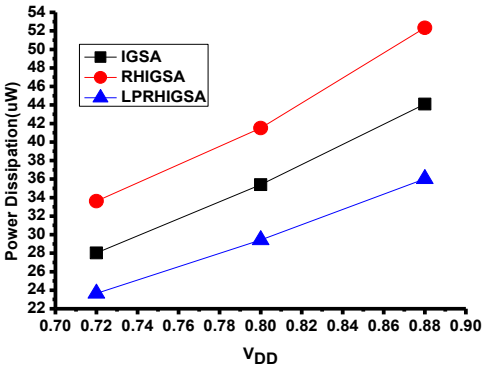

Fig.15 Power dissipation against variation in supply voltage.

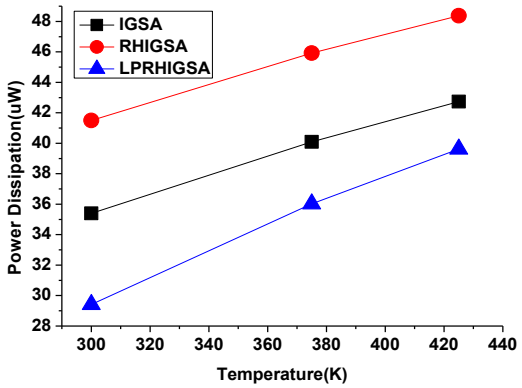

Fig.16 Power dissipation against variation in temperature in Kelvin.

Waveforms for total power dissipation at different temperatures for IGSA and RHIGSA are as shown in Fig.17. It can be observed that the switching power significantly increases with the rise in temperature from 300K to 375K.

After the sensing operation, back gate of the critical transistor connected to logic 'high' output is not completely switched 'off'. This results in a short circuit current. From Fig.17 It can be observed that the short circuit current is present in all types of sense amplifiers. Dynamic power dissipation for LPRHIGSA is less as compared to RHIGSA and IGSA.

Table-4 Power dissipation for variation in back gate oxide thickness when V_{dd}=0.8V

Power dissipationFor(in µW)	t_{box}/t_{fox} Ratio					
	1.0	1.2	1.4	1.6	1.8	2.0
IGSA	42.76	41.62	40.28	38.93	37.15	35.40
RHIGSA	48.73	46.01	45.73	44.66	43.54	41.50
LPRHIGSA	36.62	34.35	33.13	31.89	30.65	29.42

Table-5 Power dissipation for 10% variation supply voltage when t_{box}/t_{fox} Ratio=2

Power dissipation For(in µW)	10% V_{dd} Variation		
	0.72	0.80	0.88
IGSA	28.02	35.40	44.10
RHIGSA	33.62	41.50	52.33
LPRHIGSA	23.66	29.42	36.03

Table-6 Power dissipation for temperature when V_{dd}=0.8V and t_{box}/t_{fox} Ratio=2

Power dissipation For(in µW)	Temperature Variation(in Kelvin)		
	300	375	425
IGSA	35.40	40.09	42.74
RHIGSA	41.50	45.92	48.38
LPRHIGSA	29.42	36.02	39.62

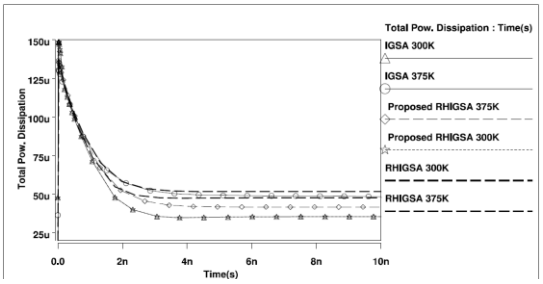

Fig.17 Effect of temperature on Total Power Dissipation

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4. CONCLUSION

A new low power, process parameter tolerant sense amplifier is proposed. The proposed design is introduce output controlled tail Fin-FET rather than SEN controlled, Which dynamically control the threshold voltage of Fin-FET. Whenever, sense amplifier start read operation threshold voltage of stack Fin-FET becomes lower then as operation goes to end threshold voltage of stack transistor becomes higher. So, the resultant power dissipation reduced up to 20.11% compare to RHIGSA (16.89% compare to IGSA). Sense delay of proposed design is similar like RHIGSA and reduced up to 40% for IGSA. Similarly Layout Area of proposed design is similar like RHIGSA and increased up 75% for IGSA.

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