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Curvilinear Structure of HFET for Low Frequency Noise Measurements

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Abstract: A combination of the wide bandgap (3.3 eV of GaN to 6.3 eV of AlN) which leads to high breakdown fields. Therefore, output power density has become a very important figure of merit for GaN/AlGaN HFETs. Extensive research has been performed to improve the output power density from 1.1 W/mm in 1996 [1] to the state-of-the-art value of 9.8 W/mm in 2001 [2]. In order to get high power density, the product of n_s and electron mobility, $\square_n$, should be maximized. Increasing the Al mole fraction in the AlGaN cap layer will lead to higher , but will drop due to alloy disorder scattering and the crystal quality may degrade as well (e.g., density of impurities is higher.

Keywords: Curvilinear Structure, HFET.

I. INTRODUCTION

A combination of the wide bandgap (3.3 eV of GaN to 6.3 eV of AlN) which leads to high breakdown fields. Therefore, output power density has become a very important figure of merit for AlGaN/GaN HFETs. Extensive research has been performed to improve the output power density from 1.1 W/mm in 1996 [1] to the state-of-the-art value of 9.8 W/mm in 2001 [2]. In order to get high power density, the product of n_s and electron mobility, $\square_n$, should be maximized. Increasing the Al mole fraction in the AlGaN cap layer will lead to higher , but will drop due to alloy disorder scattering and the crystal quality may degrade as well (e.g., density of impurities is higher.

A system for low frequency noise fluctuations measurements on semi-conductor devices is analyzed. The system uses a novel, programmable current amplifier, which enables computer-controlled device biasing for static and noise characteristics measurements at the currents varied by up to 9 orders of magnitude, with a corresponding programmable gain variation. GaN-based HFET is interesting research. Such current dynamics is needed for extraction of device parameters. The system's application for that purpose is illustrated using the low frequency noise, LFN, results obtained on HFET gate dielectrics. A high peak current 0.9 A/mm at V_{GS} = 1.75 V was obtained.

The insertion of the thin AlN (approx. 1 nm) curvilinear layer simultaneously improves the sheet charge density and mobility compared with the conventional AlGaN/GaN heterostructure having equivalent AlGaN parameters.

II. DEVICE STRUCTURE

Fig. 1 shows the schematic cross section of the AlGaN/AlN/GaN structure. The samples studied in this paper were grown by metal organic chemical vapor deposition (MOCVD) on semi-insulating SiC substrates. The new curvilinear structure consists of an 120-nm [3] AlN nucleation layer, a 1.25□ m semi-insulating GaN

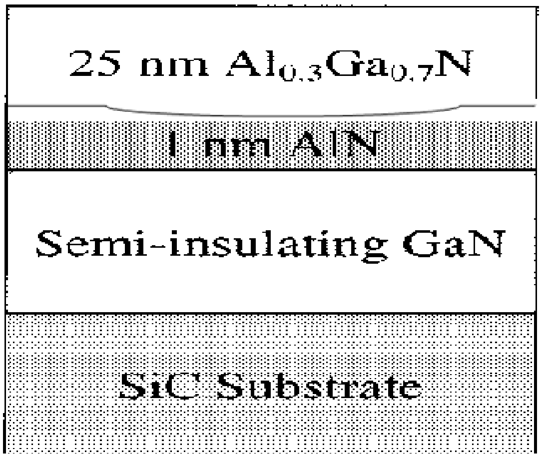
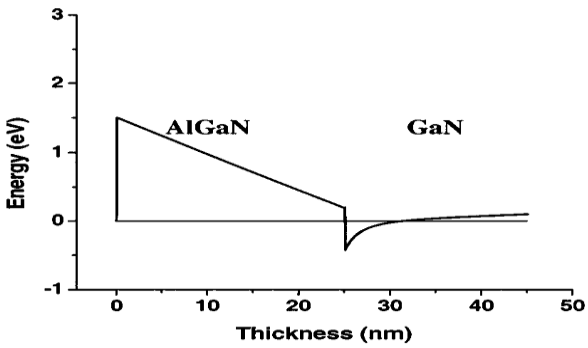


Fig.1. Schematic cross section of an AlGaN/AlN/GaN HFET

layer, a 1-nm AlN interfacial layer and a 25-nm $Al_{0.3}$ $Ga_{0.7}$ N cap layer. The band diagrams for the new AlGaN/AlN/GaN structure and the standard AlGaN/GaN structure simulated by SILVACO (TCAD) described here, are shown in Fig. 2. Fig. 2(b) shows that the insertion of the thin AlN curvilinear layer produces a larger effective □ E_C, is due to the polarization-induced dipole in the AlN layer.



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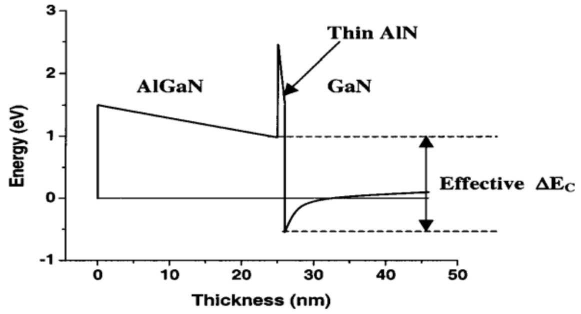

Fig.2. Schematic conduction band diagram of:
(a) Conventional AlGaN/AlN HFET,
(b) Novel AlGaN/AlN/GaN HFET. Dipole in AlN increases the effective □ E

The primary advantage of the 1-nm AlN Curvilinear layer is the decrease in alloy disorder scattering leading to an increase in mobility. This is because the electron penetration into the AlGaN is reduced due to the higher □ E_C.

As reported in [4], the decrease in alloy disorder scattering improves low temperature two-dimensional electron gases (2DEG) mobility. Additionally, considering the large 2DEG densities attainable in this materials system, alloy disorder scattering can play a significant role in room temperature mobility values [5]. Meanwhile, the larger □ E_C results in a small increase in 2DEG concentration.

A series of HFET samples were grown: a) conventional structure: 23-nm $Al_{0.3}$ Ga_{07} N / GaN; b) novel structure with unintentionally-doped (UID) cap AlGaN: UID 23-nm $Al_{0.3}$ Ga_{07} N / 1 nm AlN/GaN; c) novel structure with Si-doped cap AlGaN: 18-nm Si-doped $Al_{0.3}$ Ga_{07} N /5 nm UID $Al_{0.3}$ Ga_{07} N /1 nm AlN/GaN. Doping density is approximately 1 x 10^{18} $cm^{□3}$. The sample with Si-doped AlGaN cap layer showed the best performance.

The sheet charge density 1.33 x 10^{13} $cm^{□2}$ and room temperature mobility 1633 cm^2 /V-s are large improvements over the standard AlGaN/GaN structure. Low temperature (78 K) hall measurement showed that the charge at low temperature was very close to that at room temperature. The role of the silicon and corbon dopant is still under investigation.

III. DEVICE PERFORMANCE

Devices were fabricated on a sample SILACO. Ti/Al/Ni/Au (20 nm / 220 nm / 55 nm / 45 nm) ohmic contacts were evaporated and annealed at 870^0 C for 30 s. Mesa isolation was accomplished with Cl_2 reactive ion beam etching. Ni/Au (30 nm/300 nm) was evaporated for gate metallization.

The final processing step was a 100-nm Si_3N_4 passivation layer, which has been shown to eliminate DC to RF dispersion.

Typical DC output current-voltage characteristics of a 0.15-mm-wide Curvilinear HFET with gate length L_G = 0.6 □ m and gate-drain spacing L_{GD} = 1.8 □ m are shown in Fig. 3.

The peak value of extrinsic transconductance, g_m , is approximately 200 mS/mm near V_{GS} = □ □ 1.5 V.

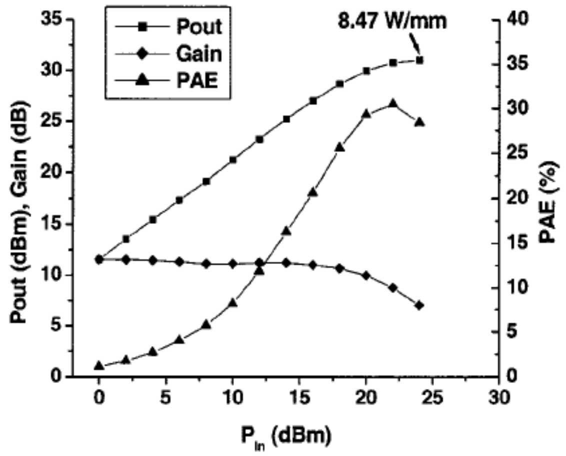

Fig.3. I–V characteristics of an AlGaN/AlN/GaN curvilinear HFET

The Schottky gate turn-on voltage is approximately 1.5 V and gate-drain breakdown voltage is typically 70~80 V. The ohmic contact resistance range was 0.5 – 0.7 □ -mm. No stability problem was observed, compared with the conventional AlGaN/GaN HFET.

The LFN is known to increase in amplitude as the device proportions are changed. Each novel generation of microelectronics devices requires, then, taking some measures towards the LFN reduction. They serve not only for providing standard noise transistor parameters for device simulation, hut also can we used for extracting some important substantial parameters of the transistors. High noise is clearly an unwanted feature in electronics devices, however the LFN-based parameter extraction methods are easier in nosier devices. Taking a MOSFET family as an example, we recall that the power spectral density, PSD, of drain current, I_d. fluctuations can be used for evaluating the surface density located near the gate dielectric interface [6]. This method gains in importance, as other methods used for this purpose, such as charge pumping, become unreliable in downscaled devices, possessing ultra thin gate oxide insulation. In such devices high leakage currents at relatively low gate voltages, V mask the displacement currents. The leakage affects less the LFN measurements, which can he also carried out at lower V, values, in order to reduce leakage.

The improved interest in the LFN measurements in transistors has brought about a development in equipment construction [7]. However, to our knowledge, the systems available now at the market [7] are designed mainly for LFN measurements at relatively high currents. That can he adequate for comparative transistor tests, hut is insufficient for extraction of certain LFN or structure parameters that require considerable current dynamics, of several orders of magnitude.

Programmable point probe noise measuring system

The electronics and software used in the programmable point probe noise measuring system, SILVACO (TCAD) described here, has been developed to comply with the

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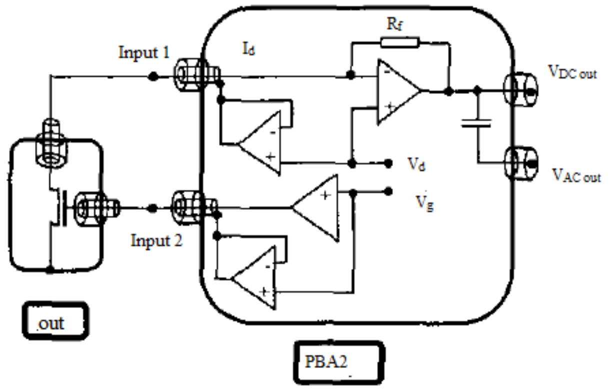
basic requirements that an automatic LFN measuring system should meet. The SILVACO (TCAD) (i) features a low-noise point-probe wafer-level contacting, (ii) shows no computer-generated noise, and (iii) provides a programmable data acquisition and storage.

Figure 3 presents a schematic diagram of the essential element in the TCAD electronics, a double-input, programmable biasing amplifier, PBA2, here shown in a configuration adapted for the HFETs. Two inputs of the PBA2 can he remotely biased and the current flowing through Input 1 is measured, with the software controlled DC-gain, $G_{DC} = R_f$, selection, assuring the optimal device noise signal/system noise ratio. Input 2 provides Vg, with no current measured (option). Both inputs are triaxial (standard 3-bayonet triax receptacles), with guard for the probes outer shells. For this reason the PBA2 can be also used with standard semiconductor test fixtures.



A schematic diagram of the programmable biasing amplifier, PBA2, used as a current amplifier for the drain current and for biasing the gate of a curvilinear HFET. Standard three-terminal or two terminal devices can be inserted in the device under lest (DUT) module.

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