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Optimized Design of Active Pixel Sensor using CMOS 180 nm Technology

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Abstract: In this paper, an Active Pixel Sensor of CMOS Imager using 5T architecture has presented. The sensor has been designed in 180nm CMOS technology. This CMOS Image Sensor consist of pixel that act as basic unit cell, called picture element that employs number of NMOS transistors with single reverse bias p-n-junction diode. The schematic, layout and simulated results of Pixel have been presented and described. The pixel designed in this paper occupies the area of (10X10) um^2. There are such parameters of Pixel have been modified- Well capacity, Conversion gain and Fill factor. The calculated results of sensor employs well capacity of (55935 e^-), Conversion gain of (39.5 µV/e^-) and Fill factor of (45.5%).

Keywords: CMOS Image Sensor (CIS), Active Pixel Sensor (APS), Photodiode, Image Sensor, CMOS.

I. INTRODUCTION

With large scale integration in CMOS technology, the rapid development has seen in CMOS Image Sensor due to its number of advantages than CCDs. These are such applications that requires high speed Image Sensor i.e. fluorescence, time of flight imaging, spectroscopy and radiation therapy [1]. The CMOS Active Pixel Sensor (APS) with intra pixel charge transfer was first introduced by Fossum at JPL in 1993. The Backside illumination and photodiode was suggested in 1994 to improve the performance of Image Sensor. Since CCD photodiode required high transfer gate to reduce the barrier by making complete transfer of charge, the photodiode with CMOS Active Pixel Sensor was challenging technically. The integration of CCD photodiode into CMOS photodiode was first proposed by JPL and Kodak, in which Kodak provided low voltage implementation of photodiode [2].

In this technological world, the demand for CMOS devices increasing rapidly and became popular due to occupying less area with long life time by optimizing parameters [3]-[5]. A complete CMOS Imager consists of pixel array, row decoder, column decoder and Image Sensor processors. To improve sensor performance and to reduce cost, the optimization of pixel array and other modules takes place [6]. CMOS Image Sensor (CIS) have huge demand in the market of electronic imaging system because of its low cost, low power consumption and System on chip integration capability. CMOS Image Sensors are categorized into two groups- Active Pixel Sensor and Passive Pixel Sensor. In case of 3T Active Pixel Sensor, the photo-generated charge carriers are collected at photodiode capacitance (C_{PD}) and convert to voltage on the same node. The converted voltage transfer to the output terminal via source follower and row select transistor. The operation for 4T is quite similar to 3T, but the difference is that the charge storage node and conversion node are different in case of 4T architecture. After 4T, 5T architecture comes into focus. The only difference is between both is by using two reset transistors in case of 5T architecture. The first reset transistor is to reset the photodiode and another is to reset the floating diffusion node [7]. The CMOS Imager can be voltage mode and current mode. Current mode of CMOS Imager have disadvantage of poor linearity and high fixed pattern noise as compare to the voltage mode CMOS Image Sensor [8].]. The Image Sensor of high charge collection efficiency with better conversion gain is often required by scientific, commercial and consumer applications [9]. The image sensors with high resolution and small pitch realized for digital cameras and mobile phone cameras respectively. The technologies for Imager have to be developed without increasing die size and optical sizes due to cost constraints [10]. The innovative circuit design has led in CMOS Image Sensor (CIS) which are capable to operate at more frame per second with pixel pitches down to scale. Improving CMOS technology is made to scale down the feature size, while making this, the fill factor of CMOS Image Sensor is comparable to CCDs.

The requirements of high performance CMOS Image Sensor designed in CMOS process depends on the applications. For example- High sensitivity required by stroboscopic while low dark current is required in Biological fluorescence applications [11]. CMOS APS (Active pixel sensor) is designed to get better scalability for efficient array and high readout speed than Passive pixel sensors. In CMOS Active Pixel Sensor, the pixel is constructed of two functional parts. The first part consist

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of geometrical shape of photodiode: act as active area to integrate incident illumination energy and convert that energy into charge carriers in silicon substrate. The second part described by control circuitry of NMOS transistors for readout operations.

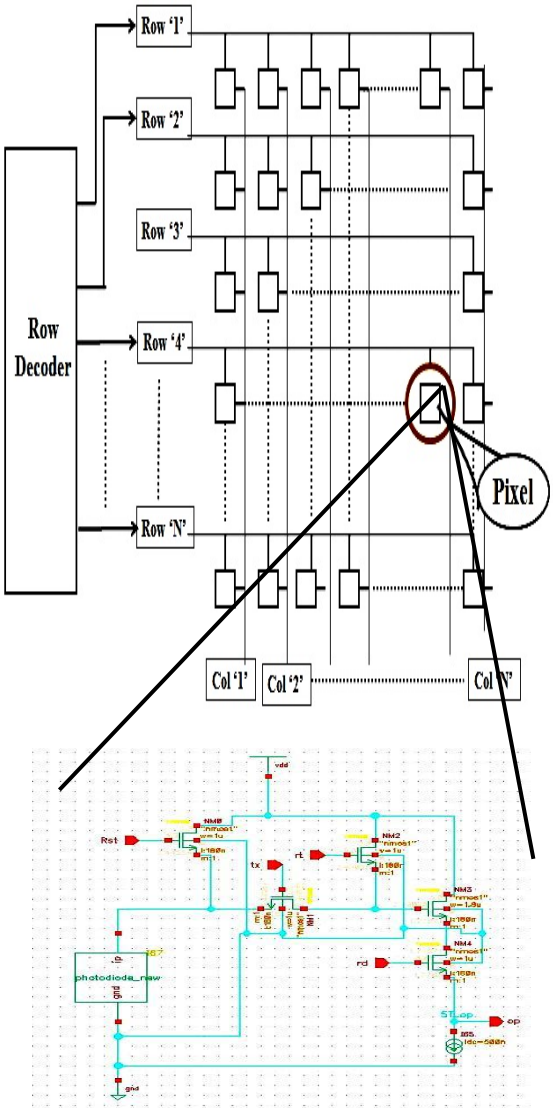

Fig. 1. CMOS Image Sensor block

The above figure shows the arrangement of array in CMOS Image Sensor. The array consists of number of pixels with Row '1', Row '2' up to Row 'N' connected to row decoder having 'N' outputs and these are responsible to connect each and every rows of pixel array during readout period. The output of pixel is taken via column lines (Col '1', Col '2' up to Col 'N') by selecting their respective rows.

II. DESIGN OF PIXEL CIRCUIT

In imaging technology, the pixel is unit cell or used as picture element which integrates the charge generated by incident illumination during exposure and produce output voltage in read out duration [12].

A. Schematic Description

The design of Pixel consists of number of transistors with single reverse bias p-n-junction diode. Since there is no requirement of N-well in NMOS transistors, it consumes minimum area. Due to the feature of area efficient in NMOS transistor, these are used in Pixel architecture.

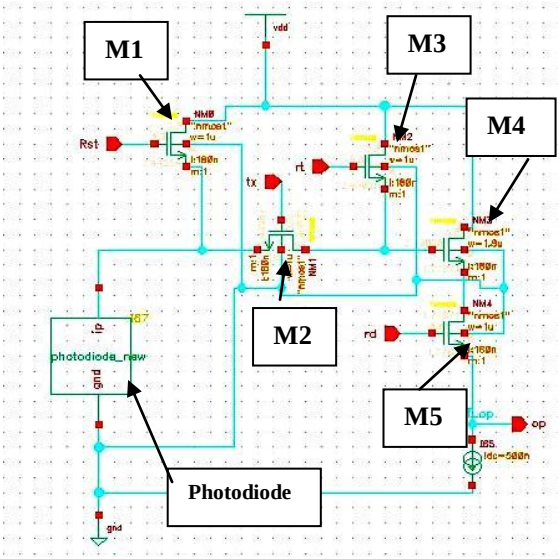

Fig. 2. Pixel circuit

The above figure shows the architecture of 5T pixel, which is extension of 3T and 4T pixel architecture to solve the issues occurred in those architecture. The 3T pixel employs three transistors (Reset, Source follower and Row select) with one photodiode, in which sense node (to sense the illumination) and conversion node (to convert charge to voltage) are same.

Due to this reason, the pixel bucket capacity and conversion gain are trade off to each other, but both parameters are important to produce better image by making efficient pixel. To solve the issue of well capacity and conversion gain, 4T pixel architecture consist of separate sense node and conversion node. In 4T design, the transfer gate is placed between photodiode and gate of source follower (floating diffusion node) to reduce noise by making complete transfer of charge from photodiode node to floating diffusion node during exposure mode.

Because of using single reset transistor in 4T pixel to reset photodiode node and floating diffusion node, the 5T pixel architecture have designed in this paper. In this design, pixel consists of one extra reset transistor (M3) at floating diffusion (FD) node to reset this node. So, there are five transistors in this design i.e. M1 (Photodiode reset transistor) to reset photodiode, M2 (Transfer gate) to charge from photodiode to floating diffusion node, M3 (Floating Diffusion reset transistor), M4 (Source follower) act as buffer, M5 (Row select transistor) to pass the output to column line by selecting row. Due to adding this reset transistor at FD, the double sampling operation takes place in 5T pixel architecture.

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B. Operation of circuit

The CMOS Image Sensor (CIS) employs pixel's operation take place in three modes i.e. Reset mode, Integration mode and read out mode sequentially. The 5T pixel architecture consists of four control signals (Rst1, Rst2, TX and RD). Initially, Reset mode takes place. During this mode, Rst1 and Rst2 (control signals of reset transistors) are high to reset photodiode and floating diffusion node respectively. At the same time, the RD (control signal of row select) is high to take out reset value.

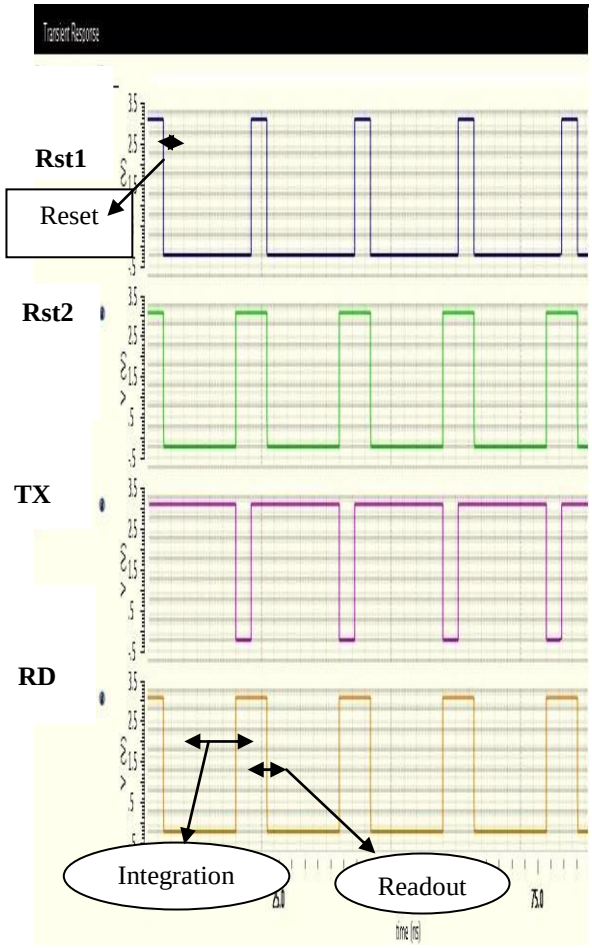

Fig. 3. Waveform for control signals

Next, Integration mode takes place. During this mode, the control signals (Rst1 and Rst2) are low, TX (control signal of transfer gate) is high for charge transfer and control signal RD becomes low because no signal is take out in this duration. At the end, Read out mode occur. During this mode, Row select transistor is high to pass pixel value (obtained by integration) at column line and control signal Rst2 is also high to make double sampling operation. After Read out mode, the all three modes repeated sequentially for all rows and output is taken out via column bus.

C. Layout of Pixel

The layout of pixel is shown in figure (4). This layout is designed in 0.18um CMOS (Complementary Metal Oxide Semiconductor) technology. The layout of Pixel consists of five NMOS transistors (M1, M2, M3, M4 and M5) and photodiode. In this design, the scale of pixel is (10X10) um^2. Within this scaling of pixel, the area occupied by photodiode is (7X6.5) um^2. The photodiode area in pixel defines the fill factor parameter which is the ratio of area occupied by photodiode to area of Pixel.

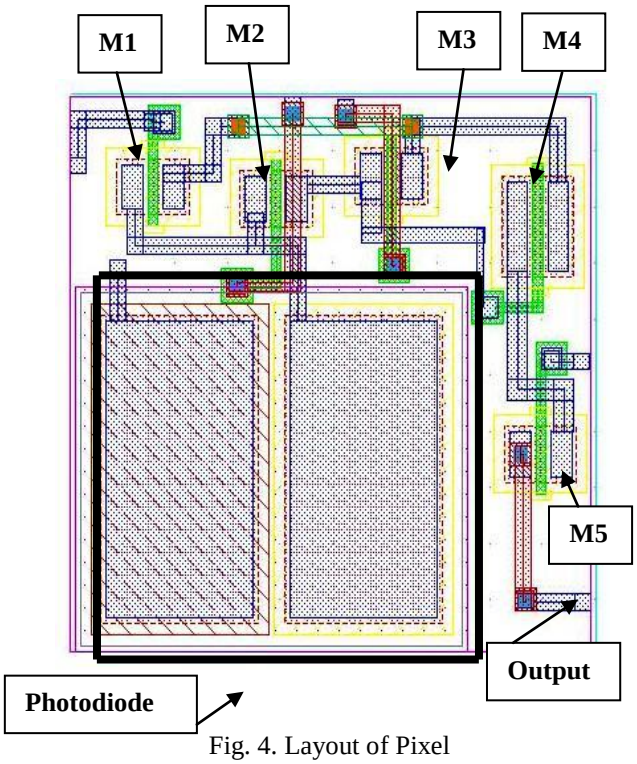

Fig. 4. Layout of Pixel

III.SIMULATION RESULTS

The Simulation of pixel is performed using spectre in Cadence virtuoso platform. The simulation results are based on 0.18um CMOS technology.

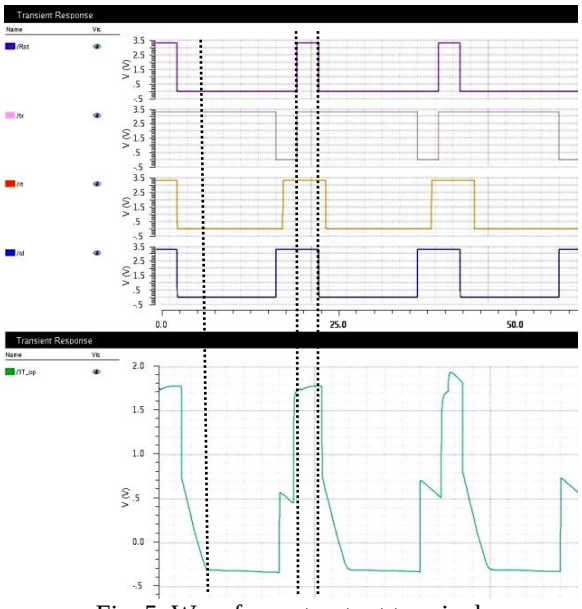

Fig. 5. Waveform at output terminal

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The fig.5 shows the waveform obtained at the output of 5T design. There are two values obtained at the output terminal due to reset and integration phases. The two values are passes via column bus by selecting row select line.

TABLE I
Comparative results of Pixel

Parameter	Paper [1]	This work
Technology (µm)	0.35	0.18
Number of transistors per pixel	3	5
Pixel Size (μm^2)	(15X15)	(10X10)
Fill factor (%)	42	45.5
Full well capacity (e^-)	50320	55935
Conversion Gain at FD ($\mu V/e^-$)	25	39.5

IV. CONCLUSION

In imaging field, the CMOS Image Sensor has proved to be very promising technology for several applications to produce the better quality of image. The measured performance of 5T Architecture have been presented and compared to 3T Architecture. It improves (11.1%) of well capacity, (3.5%) of Fill factor and (58%) of conversion gain.

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BIOGRAPHIES

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