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A Survey of Different Adiabatic Techniques for Low Power

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Abstract: This paper describes about different adiabatic logics are used which are all used to provide low power. Adiabatic techniques, such as clocked CMOS logic, latched pass transistor, single phase recovery logic, adiabatic array logic, reversible logic, dual rail logic, adiabatic inverter, pipeline scheduling, CEPAL logics are discussed briefly and comparatively studied those techniques to reduce the power consumption, improve speed of the operation and to minimize area overhead. Different tools are used to design the low power circuits as Microwind, Tanner, and HSPICE.

Keywords: Adiabatic logic, Low power consumption, High speed, Minimum area overhead.

I. INTRODUCTION

In digital system power dissipation is one of the major challenges in recent years. Nowadays low power design is used, due to its emerging demand on compactable electronics devices. Over the past few decades, design of low power techniques are used, because of rising cost of energy, increase in sensitivity, lower consumption of power. High power consumption results from increased number of transistors on the die, increased overall capacitance higher operating frequencies and increased overall resistance. Power consumption in digital electronics circuits should be reduced by using several adiabatic logics. When the constant voltage scaling rules were applied there is maximum power dissipation but in adiabatic logic constant current supply is used or varying voltage supply so power dissipation is reduced. Adiabatic techniques are used to reduce consumption of energy during process of switching. Energy from the load capacitance is recycled to reduce consumption of power. Reversible logic is implemented in CMOS which controls the current flows through the circuit so that energy dissipation is decreased. Reversible logics are used in adiabatic circuits to conserve energy. Adiabatic circuits are also known as low power circuits.

A. Two rules are used in adiabatic circuits to reduce dissipation,

- Never switch ON a transistor when voltage is supplied from source to drain.
- Never switch OFF a transistor when current flows through the circuit.

B. Motivation of low power circuits

- Long life batteries operations
- Complexity increases but energy remains same
- Complexity in high speed devices
- Weight, size and cost reductions
- Noise immunity

C. Adiabatic logic circuits are,

1. Partially adiabatic circuits:

- Some energy is recovered

2N2P / 2N-2N2P
CAL (Clocked CMOS Adiabatic Logic)
TSEL (True Single Phase Adiabatic)
SCAL (Source-coupled Adiabatic Logic)

2. Fully adiabatic circuits:

- Dissipate less energy and very slow

PAL (Pass-transistor Adiabatic Logic)
Split-level Charge Recovery Logic (SCRL)

This paper is arranged as follows. Section II contains detailed explanations about literature review. Section III comparatively describes about the techniques used in various papers with their advantages and description about applications. Section IV end with conclusion.

II. RELATED WORKS

A. Clocked CMOS Adiabatic logic

CCAL technique is used here to reduce consumption of power. Various adiabatic logics such as clocked CMOS, Eight level inverter chain CCAL, QSERL are compared with CCAL technique. In Clocked CMOS logic gate structure is used for this design. It has static logic and tristate output which is managed with help of ϕ. function of this technique based on ϕ which is showed in table.1.

TWO DIFFERENT STATES OF OPERATION

ϕ=1	Both M_1, M_2 in active state	pFET, nFET Connected to output
ϕ=0	Both M_1, M_2 in cut off state	FET logic arrays are not connected to output

In clocked CMOS adiabatic logic consist of two parts, CMOS logic part which acts as logical evaluation part and clock control part that is used to control connection between logic part and output. Two complementary sinusoidal power supplies are used (p_c,p_{c_b}). NOR gate CCAL is used in this technique. It consists of two stages, evaluation and hold.

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Adiabatic switching uses resonance LC driver instead of DC power supply. Based on increase in time, energy dissipation becomes low. CCAL is compared with QSERL technique. CCAL has two advantages over QSERL, high operating frequency upto 500MHz and low power dissipation. It saves energy upto 40% at 200MHz and 15% of energy at 500MHz [2].

TABLE I :OPERATION OF EVALUATION AND HOLD MODE

Evaluation	Hold
P_c –High cycle, p_{c_b} –low cycle	P_c –low cycle, p_{c_b} –high cycle
M_1, M_2 –ON state	M_1, M_2 –OFF state
pFET, nFET - Connected to output	pFET, nFET –Not connected to output. Output is hold until P_c goes to high cycle.

B. Latched pass transistor adiabatic logic

Low power design has important problems in system on chip (soc) and VLSI design areas which will dissipate energy low power than static CMOS logic. Latched pass transistor adiabatic logic and energy saving design for low power applications. On comparing to other pass transistor adiabatic logic, LPAL will provide power saving upto 44%.

Adiabatic switching uses charging and discharging method in which load capacitor is used to load and unload the power by using dynamic power source.

Conventional CMOS logic uses abrupt voltage drop when the input state changes from high to low. When the input is high, the left transmission gate will be in ON state and right transmission gate will be in OFF state then C_L will charge. when input goes to low, then left transmission gate will be in OFF state and right transmission gate will be in ON state so, the C_L discharge the power to ground through pull down transistor.

Pass transistor adiabatic logic has two phase, evaluation phase and recovery phase. V_{pc} produce electric charge that will generate a conduction path from V_{PC} to NMOS logic block. When V_{pc} moves to V_{DD}, the output state will be valid. During the recovery phase the output state will be invalid.

LPAL is made by using PAL and two mode selection transistors. PMOS mode select is placed between the V_{pc} and cross coupled two PMOS transistors. The NMOS mode selection transistor is placed between the V_{pc} and two NMOS cross coupled transistor.

When mode= V_{DD}, LPAL act as PAL gate. Mode=0 means, the mode selection will disconnect the clock and transistor circuit. Using LPAL mode=0, energy loss in adiabatic will be reduced.

The simulation result for adiabatic logic at 5MHz frequency and 0.1pf load capacitance.

ENERGY CONSUMPTION OF ADIABATIC LOGICS

Logic	Energy consumption
PAL	459.2pJ
LPAL	257.6pJ

Finally, LPAL can save 44% of energy than PAL circuit [3].

C. True single phase energy recovering logic

Dynamic logic families achieve low energy dissipation but it uses multiple phase clocks to control cascaded gates. It cannot be used for high speed design instead of clock skew management problems. True single phase energy recovering logic circuit uses single phase clock scheme. Energy recovery will be in terms of energy efficiency and operating speed. TSEL address dissipates half of the power at 280MHz.

In adiabatic logic, when input is high, half of the input is given to PMOS transistors equivalent resistor and another half of the input is given to the load capacitor. When input is low, then another half stored in the capacitance will be given to PMOS transistor-resistor. The 2N-2N2D adiabatic logic uses diodes. The diode will generate lower bound of energy.

In 2N-2P, 2N-2N2P does not have any diodes and it uses four phase clocks for controlling cascading gates, but it will produce non-adiabatic switching event occurs during the longer interval in the evaluation phase.CAL circuits achieve half the throughput of 2N-2NAP circuits [8].

D. Adiabatic array logic

Adiabatic logic uses digital circuit design for reducing power. Adiabatic logic is used to design fundamental logic gates such as NOT, NAND, NOR and XOR which will generate improved power dissipation than static CMOS logic style.

The simulation results were carried out by using NI-multisim software with 0.18µm, 1.8V CMOS standard process technology for frequency ranges between (200-800) MHz.

Conventional static CMOS logic uses DC power supply and it can be replaced by trapezoidal/ sinusoidal power source to reduce adiabatic energy loss.

Transition time is inversely proportional to energy loss. When the time interval between signals is equal, the voltage drop is less so, power dissipation will be lower. In evaluate phase, the outputs are evaluated corresponding to the input state, during the hold state, the output is maintained and applied to the cascaded circuit.

In recover phase, the energy is recovered and given back to the power source. Finally wait state is used for avoiding asymmetry. From this adiabatic array logic power dissipation is very less compared to 2PASCL [9].

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E. 4:1 Multiplexer using an efficient reversible logic
The power dissipation is more in the conventional CMOS logic. The multiplexer is designed by using both conventional CMOS logic and adiabatic logic. PFAL and ECRL is one of the adiabatic techniques which are used to reduce the power dissipation by using multiplexer. The power dissipation will be reduced and it is done for different frequency range. This type of reduction technique is used for memory designing in high performance low power circuits and various high end processors [1]. The results of circuits design with different frequencies are shown in below table,

TABLE : II RESULTS OF DIFFERENT CIRCUITS AT VARIOUS FREQUENCY RANGE

Frequency	**4:1 MUX (CMOS)**	**4:1 MUX (ECRL)**	**4:1 MUX (PFAL)**
16MHz	932µw	23.65 µw	31.76 µw
20MHz	932 µw	23.35 µw	23.25 µw
25MHz	932 µw	20.06 µw	40.24 µw

F. Dual rail adiabatic logic
The generation of heat in the conventional logic circuit and the effect of differential power are more. CMOS reversible logic is used to reduce the power dissipation due to switching and capacitor where the current flows through the circuit is controlled. By using dual rail adiabatic logic there is reduction in average and differential powers and it allows design reuse in encryption and decryption. There are two rules in dual rail method, they are

1. Reduce leakage power:
The voltage across the transistors must be minimized, when the transistor is ON.

2. Reduce leakage current:
The voltage across the transistors must be minimized, during any switching event.

ESPRESSO heuristic algorithm is used for reducing the size of circuit by minimizing Boolean functions. There is 36% improvement over the existing logic. Adiabatic S-box reduces the imbalances in energy, compared to previous benchmark with average improvement of 65%. It can able of reverse decryption and forward encryption with reduced overhead, which allows effective reuse of hardware. In dual rail adiabatic logic there is an enhancement in differential power than single rail and conventional logic. There is an effective reduction of DPA attacks by using S-box. Dual rail adiabatic logic is mainly used in security applications with low frequency (smart cards) [5].

G. Two level pipeline scheduling
In adiabatic circuits the existing scheduling algorithm is unsuitable. ILP (Integer Linear Programming) and heuristic scheduling is used for high level synthesis. Based on the four phase adiabatic logic, the phase clock controlled evaluation of each logic stage influences automated design tools. The main advantages of using this scheduling algorithm are low energy dissipation and increase the speed of operation. Both ILP and heuristic pipeline schedule using minimum number of resources but in ILP the buffer length is decreased. It is mainly used in signal processing application [4].

H. Low power adiabatic inverter
In PFAL logic, a latch was made by two PMOS and NMOS transistor. In modified PFAL pull up and pull down networks of NMOS and PMOS are interchanged. Here the power supply V_{DD} is used whereas in conventional technique power clock is used. Efficiency is improved with help of cross coupled latch connection. The improved low power characteristics and the less power dissipation obtained as 70%. The delay characteristic of modified PFAL inverter is 98% better than the conventional PFAL [6]. Results of power delay product for different adiabatic inverters,

TABLE III. POWER DELAY PRODUCT OF DIFFERENT ADIABATIC INVERTERS

Inverter circuits	**Power delay product**
2n2n2p	12.98
ECRL	10.43
PFAL	7.89
Modified PFAL	0.654

I. Different Adiabatic and CMOS full adder circuits
In DSP and microprocessors full adders are one of the important components. The power dissipation occurred in CMOS full adder is comparatively higher than the different adiabatic circuits. The different adiabatic logics are,

i. Pass transistor logic (PL) based adder:
PL based adder is one of the NMOS logic style used to implement different functions. The main aim of complementary PL is to implement logic functions by using only an nMOSFET. It provides low input capacitance, high speed operation and lowest amount of power than usual static circuits, because the supply voltage is greater than logic swing of the pass transistor outputs.

ii. Transmission Gate Logic (TGL) based adder:
Transmission gate is used to implement a digital function which is similar to pass transistors. But the transmission gate logic uses nMOS and pMOS transistors where pass transistors uses only one type of transistor (either nMOS or pMOS).

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iii. Static energy recovery full adder (SERF) or 10T adder:
In SERF the pass transistor logic is used to implement the XOR and XNOR of A and B. The input signal A is inversed or complemented with help of inverter. At the output the balanced delay occurs from the realization of faster XOR and XNOR outcomes.

This leads to minimum errors in SUM and CARRY signals. The capacitance also reduced at the outputs of XOR and XNOR gates. The signal degradation at the SUM and CARRY can be reduced by drivers. The outputs generated with equal fall and rise times and the better performance as less power dissipation and driving capacities are obtained by using driver.

iv. Positive Feedback Adiabatic Logic (PFAL) adder:
In PFAL, two inverters with cross coupling and two functional blocks F and /F are used.

Normal and complemented outputs are obtained from normal and complemented inputs. With the help of n channel MOS transistors both the functional blocks are employed.

v. Transmission Gate based Adiabatic adder (TGAL):
An only clock power supply is used for the implementation of two functional blocks F and inverse of F in adiabatic adder which is based on transmission gate. Transmission gate or pass gate are used to implement the functional blocks.

Table shows the power dissipation of various adders at 50MHz clock frequency with 1.8 supply voltage, load capacitance is 20Ff [10].

TABLE IV: RESULTS OF VARIOUS ADDERS

Parameter	Adder type					
	CMOS	PL	TGL	PFAL	TGAL	SERF
Transistor count	28	22	20	38	60	10
Power dissipation (µw)	1.9	1.2	2.1	0.05	0.85	0.08

J. CEPAL technique (Complementary Energy Path Adiabatic Logic)
In the conventional static logic, ½ CV_{DD}^2 energy dissipation is occurring at every cycle. QSERL is stands for Quasi Static Energy Recovery Logic which overcomes the dynamic adiabatic logic but it suffers from hold phases in operation.

It can be avoided by adding clocked feedback keeper but still there is some power loss and area overhead. Using CEPAL technique QSERL can be overcame and eliminates the hold phases of QSERL. CEPAL technique is more efficient than CMOS [7]. Power comparison for different gates are shown below,

TABLE V: RESULTS OF VARIOUS LOGIC GATES OF CEPAL AND CMOS TECHNIQUES

Logic	P-MOS	N-MOS	Total Transistors	Average Power
CMOS-NOT	1	1	2	1.974µw
CEPAL-NOT	3	3	6	0.307 µw
CMOS-NAND	2	2	4	1.428 µw
CEPAL-NAND	4	4	8	0.491 µw
CMOS-XOR	4	4	8	3.652 µw
CEPAL-XOR	6	6	12	1.523 µw
CMOS-MUX	4	4	8	4.517 µw
CEPAL-MUX	6	6	12	2.032 µw
CMOS-D Flip flop	18	18	36	8.396 µw
CEPAL-D flip flop	30	30	60	2.228 µw
CMOS-4 bit shift register	72	72	144	32.192 µw
CEPAL-4 bit shift register	120	120	240	7.516 µw

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III. COMPARATIVE ANALYSIS OF VARIOUS ADIABATIC TECHNIQUES

Table VI shows the comparison table which describes about different techniques used in the papers, comparative study, applications of each technique.

TABLE VI: COMPARATIVE ANALYSIS OF VARIOUS ADIABATIC TECHNIQUES

Title of the paper	Techniques used	Application	Remarks
Design and analysis of 4:1 Multiplexer using an Efficient Reversible Logic in 180nm [1]	ECRL, PFAL, CMOS	Memory designing in high performance low power circuits.Various high end processors.	Power dissipation is less in ECRL and PFAL
Clocked CMOS Adiabatic Logic with Low-Power Dissipation [2]	QSERL, CCAL	High performance and energy efficient applications.	Power dissipation is less in CCAL.
Energy-saving Design Technique Achieved by Latched Pass-transistor Adiabatic Logic [3]	LPAL	Used in low power circuit design and more energy efficient.	LPAL saves 44% of the PAL energy
Two-level Pipeline Scheduling of Adiabatic Logic [4]	ILP and Heuristic scheduling	Signal processing and high level synthesis	Both pipeline schedule using a minimal number of resources.
Synthesis of Dual-Rail Adiabatic Logic for Low Power Security Applications [5]	S-box, ESPRESSO Heuristic algorithm and reversible logic	Minimal overhead occurred in forward encryption and reverse decryption	Efficient hardware reuse
A Novel Design of Low Power Adiabatic Inverter [6]	Modified PFAL inverter	Better low power characteristics	70% less power dissipation and 98% better in delay characteristics than PFAL inverter
Power Reduction Technique Using Adiabatic Logic [7]	CEPAL (Complementary Energy Path Adiabatic Logic)	Low power electronics	Better power efficiency than CMOS
True Single-Phase Energy-Recovering Logic for Low Power, High-Speed VLSI [8]	TSEL	High speed and low power VLSI design system	At high operating speed the power dissipation is low.
Low Power Design and Analysis of Fundamental Logics Using Adiabatic Array Logic [9]	2PASCL	Low power digital circuits	Power saving is high than CMOS
Power Comparison of CMOS and Adiabatic Full Adder Circuits [10]	Different adiabatic techniques such as, PL, TGL, TGAL, PFAL, SERF	Low power circuits	High transistor count

IV. CONCLUSION

Adiabatic logic has been implemented and to get a reduced power dissipation. The different CMOS and adiabatic circuits are designed and the corresponding outputs of power dissipation have shown in the comparative analysis table. In CMOS the power dissipation will be higher than the adiabatic circuits. The low power can be achieved by sustaining small potential difference across the transistors. Charge stored up in load capacitors should be recycled during conduction. Adiabatic logic attains less power and faster operation.

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BIOGRAPHIES

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