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Novel ASIC Design flow for Multi-rate FIR Filter from System Specification to Functional Verification

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Abstract: Finite impulse response filter holds important part in DSP designs. Multi-rate FIR filters specially are the integral part of the various DSP applications like speech coding, audio compression, image processing and others. In VLSI designs, especially nowadays, in SOC designs, requires efficient implementation of FIR filter. Fixed point FIR filter design is the challenging task in ASIC designs. Here, ASIC design flow for a multi-rate FIR filter is proposed from system parameters to verification. From the help of FDATOOL in MATLAB, different fixed point FIR filters are designed and RTL like MATLAB model is designed. Also, filter coefficients are optimized with common sub expression elimination technique. This model helps in optimizing HDL modeling in terms of arithmetic and verification.

Keywords: FIR filter, Multirate filtering, ASIC, SOC design, CSE, RTL like MATLAB model, functional verification.

I. INTRODUCTION

FIR filters are the integral part of the DSP based SOC. Design issues of FIR filter includes meeting of rigid spectral specifications, limiting number coefficients for speed and area optimization, speed and time delay consideration due to multiplications in next stages of filter, saturation arithmetic, etc. Careful design flow requires for such designs in starting from system specifications to synthesis [1]. RTL modeling is totally depends on coefficients derived from MATLAB modeling. The following sections describe such flow for efficient implementation.

A. Brief Introduction

We can characterize a causal FIR filter's input-output real time relationship as below;

$$Y(n) = \sum_{i=0}^{k} b_i \;\; x(n - i)$$

$$= b_0 x(n) + \; b_1 x(n-1) + b_2 x(n-2) \ldots . b_k x(n-k)$$

Where bi denotes filter coefficients and K+1 gives filter length.With applying z-transform to above equation we get,

$$Y(z) = b_0 \, x(z) + b_1 \, z^{-1} \, x(z) \ldots \ldots + b_k \;\; z^{-k} \, x(z)$$

And transfer function of the system is given by,

$$H(z) = \frac{Y(z)}{X(z)} = \; b_o + b_1 \, z^{-1} + \ldots . . + b_k \, z^{-k}$$

The figure below shows the direct form FIR filter structure from the above equation [3].

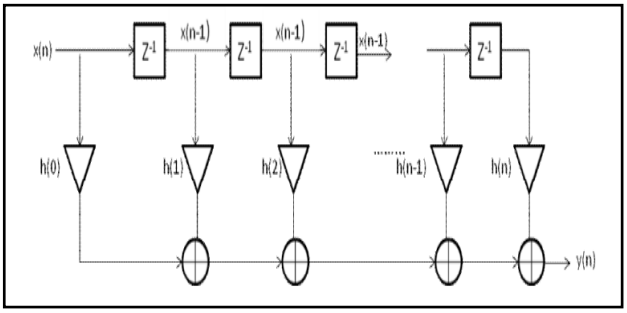

Figure 1 Direct form-I structure

B. FIR filter spectral parameters

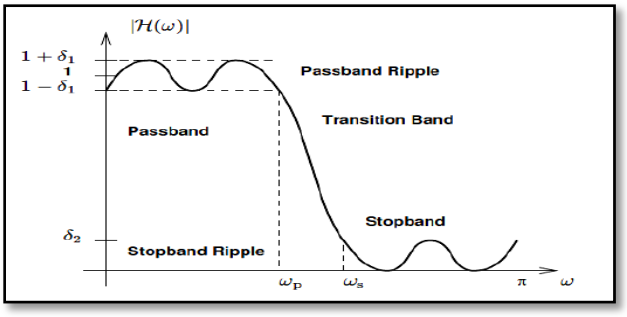

Figure 2 Spectral parameters

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Figure 2 shows the general FIR filter magnitude response. Main filters spectral parameters are pass band ripples and stop band attenuation. Next is transition width, Narrower the width, more expensive is the design. That means as more rigid spectral requirements, more will be the number of coefficients for better impulse response and so more will be the hardware need for ASIC design.

II. MULTIRATE FILTERING

A. Basics on multi-rate filtering

When more then one sampling rate required at that time multirate digital signal processing is required. By using up sampler and down sampler we can obtain different sampling rate. Up sampling will increase sampling rate also known as interpolation and down sampling will decrease sampling rate also known as decimation.

B. Multi-stage approach

One effective way of improving the efficiency of filter designs is to use several stages connected in cascade. Multi-stage design breaks our design in to two stages. It uses up-sampling of an impulse response in order to achieve a narrow transition band while only adding zeros to the impulse response (therefore not increasing the complexity). The up sampling introduces spectral replicas that are removed by the second stage filter which is a low-pass filter with less stringent transition bandwidth requirements. The multi-rate implementations of multistage designs are the most effective way of implementing.

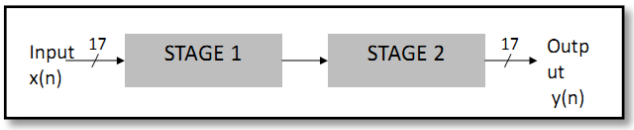

Figure 3 Two stage implementation

Figure 3 shows the two stages implementation of our multi-rate design.

III. IMPLEMENTATION FLOW

A. Matlab Implementation Flow

Figure below shows the MATLAB flow for designing the given FIR filter from the specifications. The important of the flow is that as much filter coefficients are optimized, as much HDL modeling will be the efficient during synthesis.

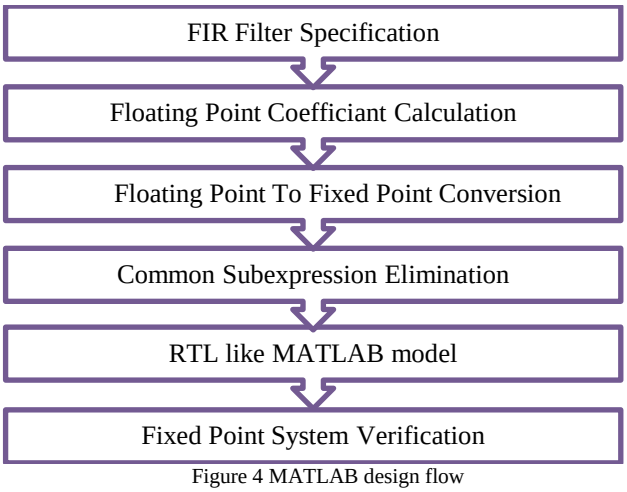

Figure 4 MATLAB design flow

B. Coefficients derivation and conversion to fixed point.

By means of FDAtool in MATLAB or by coding your filter in MATLAB script we can derive our coefficients in floating point format. As, coefficients are derived, very first task is to convert them in to fixed point format because ASIC implementation needs very less hardware cost and less instruction cycles which can not be satisfied by floating point format. The only problem with fixed point arithmetic is overflow situation because of having very narrow dynamic range. Q-format number representation is the most common one used in fixed-point DSP implementation [4]. Figure below shows the Q-15 fixed point arithmetic format which holds one bit (MSB) for sign representation and rest of the bits for magnitude. We convert any fractional number in Q-format by multiplying with 2^(Q-format value) and then take binary value. (2's complement for negative number).

C. Structure Optimization

Symmetry properties of the linear phase filter coefficients can be used for reducing the multiplication operation by half prior to that direct form structure. Figure below shows the symmetrical direct form structure, which requires half of the multipliers compared to prior one.

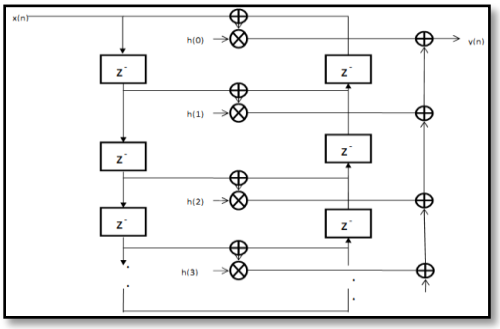

Figure 5 Linear phase direct form structure – symmetric

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D. Common sub expression elimination

Since the co-efficient are fixed in the design, the multiplier can be optimized in terms of shift and add operations. With the concept of sub-expression sharing the overall shift-add units can still be optimized[2]. This is relevant for hardware implementation to avoid costly multipliers, but may also be beneficial for software implementations. As a simple example,

y = 7x can be computed as, y = (x<<3) + x

E. RTL like MATLAB model

We can design RTL like model in MATLAB script and analyze it for filter performance. This model serves as a good practice before starting HDL modeling for RTL designing. We can verify filter functionality before actually starting coding it in HDL. Figure below shows the chunk of RTL like MATLAB modeling for example.

```
%  [10 15 39 200 254 3120 14203 56621]
reg = zeros(1, 21);

%% Implementing filter 1
  rtl_filter1_out = [];
  %  Declaring the egisters:
    for X = input_signal
       % Propagating each new input sample along the logic

for x = stim
  t41387     = reg(10) + reg(11);
  t12932_    = reg( 9) + reg(12);
  t6808      = reg( 8) + reg(13);
  t3982_     = reg( 7) + reg(14);
  t2354      = reg( 6) + reg(15);
  t1349_     = reg( 5) + reg(16) + t3982_ * 2^1;

  t91 = reg( 4) * 2^3 + reg(17) * 2^3 + t1349_ - t12932_ * 2^7;
  t321 = t41387 * 2^7 - t3982_ * 2^2 - t12932_ * 2^2;
  t37 = t45 - t91 + t41387 * 2^3 + t2354 * 2^6;
  t39 = t37 - t321 + reg( 2) * 2^2 + reg(19) * 2^2;
  t7 = x * 2^1 + reg(21) * 2^1 + t39 - reg( 1) * 2^3 - reg(20)
  y = t7 * 2^3 - t7 + t39 * 2^5 - t37 * 2^1 + t45 * 2^3 + t91 *
       2^7 + t41387 * 2^1 + t41387;

  resp(end+1) = y;
  reg = [x reg(1:20)];
end
```

Figure 6 RTL like MATLAB model

IV. IMPLEMENTATION FLOW IN RTL

After deriving fixed point coefficients in MATLAB, and RTL like MATLAB model verification, one can start RTL modeling using any HDL like Verilog or VHDL. It starts with SOC requirements in terms of power, area and speed. Various coding techniques like FSM optimization, LUT and pipelining can be used for efficient HDL designing. Figure below shows the RTL front end flow till functional verification.

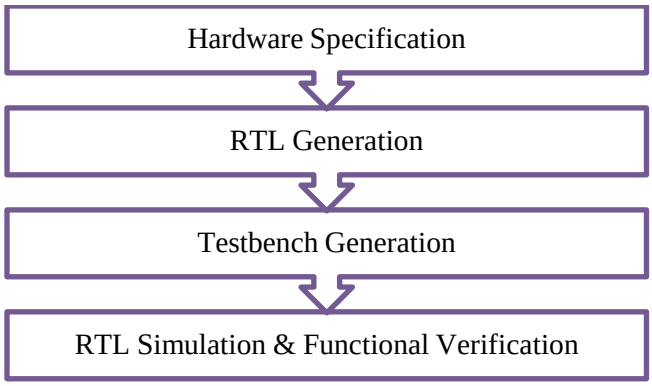

Figure 7 RTL design flow

A. Verification Plan

Proper verification plan holds an important in effective functional verification process. It saves considerable amount of time in such process. There are mainly two approaches are generally followed in DSP blocks verification. One is with MATLAB model incorporation in the verification process, and other is with incorporating c/c++ model in verification process. The generic proposed verification approach with MATLAB model incorporation is shown in the figure below. The plan includes RTL like MATLAB model results comparison with HDL designed model with test-bench environment.

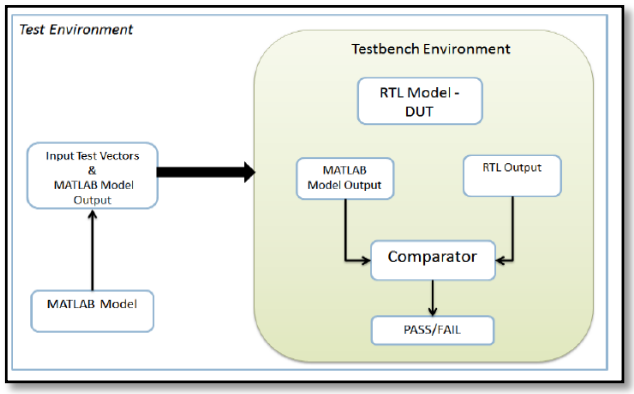

Figure 8 MATLAB model verification approach

V. CONCLUSION

The implementation of this multi-rate FIR filter starts with given MATLAB design flow. Started with single stage approach, multi-stage approach should be adopted in terms of efficient design. After generating coefficients from MATLAB, fixed point conversion should be done from floating points coefficients. For arithmetic optimization,

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symmetric direct form FIR filter structure can be used for filter realization and can reduce number of multipliers by half. Moreover, multiplier free approach is effective with the concept of common sub-sharing expression elimination. RTL design should be verified by RTL like MATLAB model approach first and then after HDL modelling, functional verification can be done by given MATLAB model verification plan.

VI. FUTURE WORK

Future scope of this work can be expanded to half band filter designing which a class of multi-rate filtering with interpolation factor of 2. Also known as Nyquist filter, this half band filters are very efficient in terms of performance and hardware costs.

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BIOGRAPHY

Heena Patel is pursuing her Mtech in Electronics and Communication from Uka Tarsadi University, Bardoli, India. Her area of interest are image processing, ASIC designs and digital signal processing.