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FPGA Implementation of Content Addressable Memory Based Information Detection System

Mayuri Soni[1], Sapana Kukade[2], Preeti Lawhale[3]

Assistant Professor, Department of E&TC Engg, PRMITR, Badnera, Amravati, India[1,2,3]

Abstract: CAM (content-addressable memory) is a specialized type of high-speed memory that searches its entire contents in a single clock cycle. We are designing generalized CAM using Dual Port RAM (random access memory) structure which will perform match operation in addition to read and write operation .The design has fast search capabilities while consuming least system resources as possible.CAM provides performance advantage over other search algorithms as searching is based on content rather than address unlike RAM. The match time of our CAM structure is faster and resources are more effective.CAM is used in application where search time is very critical. content addressable memory compare input search data against stored data and return address of matched data. Thus overall function of CAM is to take search word and return matching memory location.

Keywords: Dual Port, RAM (random access memory), CAM (content-addressable memory), match

I INTRODUCTION

A CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. We take advantages of Content Addressable Memory (CAM) which has an ability of matching mode for designing the system. The CAM blocks have been designed using available memory blocks of the FPGA device to save access times of the whole system. CAM provides a performance advantage over other memory search algorithms, such as binary or tree-based searches or look-aside tag buffers, by comparing the desired information against the entire list of pre-stored entries simultaneously, often resulting in an order-of-magnitude reduction in the search time. This increases the search performance of the information detection system which uses this method as the core system. While CAM's are widely used in many applications like memory mapping,cache controllers for central processing unit, data compression and coding etc. it primary application is fast Internet Protocol (IP) package classification and forwarding at high speed network routers and processors. The two most common search-intensive tasks that use CAMs are packet forwarding and packet classification in Internet routers. IP routing is accomplished by examination of the protocol header fields i.e. the originating and destination address, the incoming and outgoing ports etc. against stored information in the routing tables. If a match is registered the package isforwarded towards the port(s) defined in the table. On very high speed networks and huge traffic volume the task is to be performed in fast and massive parallelism. However, managing high speeds and large lookup tables requires silicon area and power consumption.

The power dissipation , silicon area and the speed are three major challenges for designers. Since there is always trade-off between them , reducing one without sacrificing the others is a is the main threat in recent research for large CAMs. The rest of this paper is organized as follows. section II introduces Design approach, reported researcher work is discussed in section III, CAM structure on FPGA is in section IV, section V presents results of proposed design and In section VI conclusions are discussed.

II DESIGN APPROACH

The main goal of paper is to design search engine on hardware system such as FPGA without increasing the detection time and system complexities .We have proposed efficient information detection system employing multimatch content addressable memory.The architecture is based on parallel structure to achieve fast detection ,accelerating the search performance ,consuming only memory resources as least system resources as possible.

III. RELATED WORK

CAM hardware has been available for decades and many research are addressed to development of high capacity and effective CAM designs at circuit, architectural and application level. A lot of projects are leaning towards "real live" application for effective algorithms for package forwarding based on CAMs and its extended version TernaryCAM (TCAM) [1]. CAM memories enhanced with "don't care" states are used for more complex project like hardware based Network Intrusion Detection and Prevention Systems (NIDPS) [8]. At "lower" level designs many papers introduce methodologies and optimization to speed , power and physical circuit resources. Authors of [2] in detail describe the principle of CAM functions at transistors and circuits level including core cells, match line and search line structures and power consumption formulation. Also power and area reducing techniques are presented on the circuit level. Practical design on architecture level is presented by [4]. The proposed CAM chip design is based on modification to the RAM chip circuit explained in [5]. fig 1 shows Dual Port RAM (random access memory) structure which will perform read and write operation. Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches

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its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found.

Binary CAM is the simplest type of CAM which uses data search words consisting entirely of 1s and 0s.

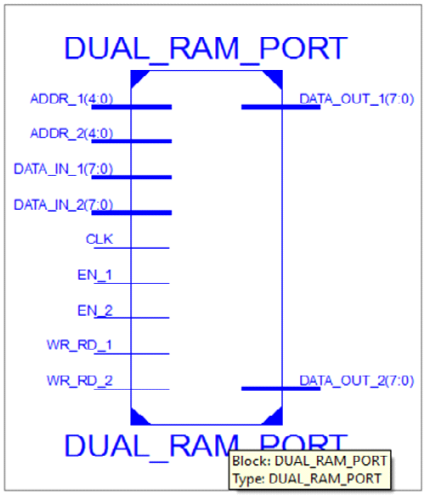
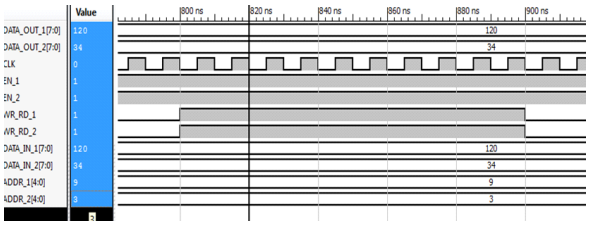


Fig 1: Dual Port RAM structure

Simulation Result:



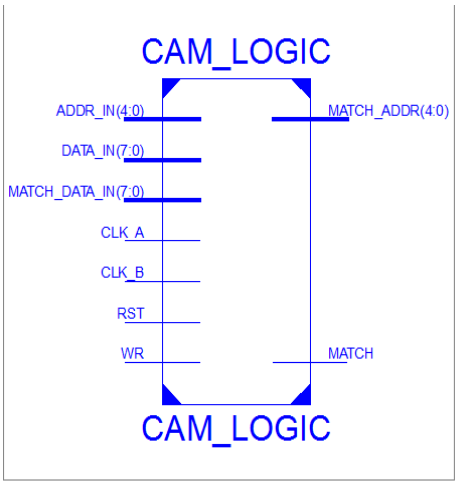
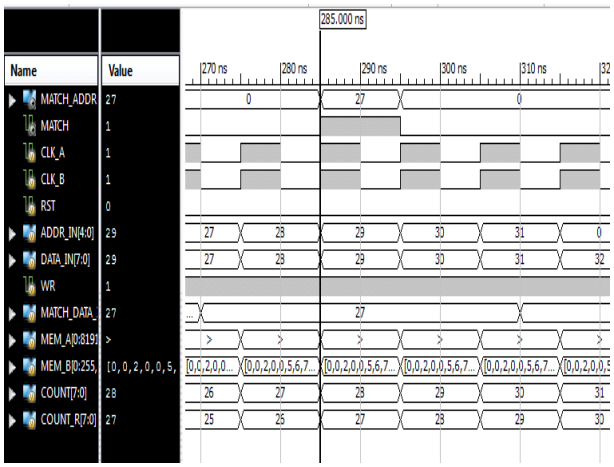


Fig 2: CAM structure on FPGA of the size 32*8

Simulation Results:



IV. CAM STRUCTURE ON FPGA

However designing CAM on FPGA hardware has also received much attention. we have implemented the CAM based on the dual-port RAM structure. Each dual-port consists of 8192 memory bits and 1024 bits for parity check codes. Port-A is used to store or erase data in the CAM and is therefore a write-only port. Port-B is used to look up matched data and is a read-only port.

Port-A would be configured to be $2^{(8+5)}$-bit address and 1-bit data for 8192-word×1-bit = 8192 bits. Port-B can be configured as 8-bit address (2^8 = 256 words) and 32-bit (2^5) data width for a configuration of 256 word×32-bit = 8192 bits. In Port-B, the address port will be considered as match data, meanwhile the data port is considered as match address. It means that, at Port-B, the 8- bit address will become 8-bit matched data, meanwhile the 32-bit data will be 32-bit match one-hot address.

Fig 2 shows CAM structure on FPGA of the size 32 word,8 bit which is defining the depth and width of CAM. Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. There are cost disadvantages to CAM however. Unlike a RAM chip, which has simple storage cells, each individual memory bit in a fully parallel CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit. Additionally, match outputs from each cell in the data word must be combined to yield a complete data word match signal.

.Here if input data matches with stored data in memory then match signal will be high and corresponding count will be matched address.This count is incremented when next match occur in memory. In this way whatever data is stored in memory ,if it matches with the input data then match signal is high.

The additional circuitry increases the physical size of the CAM chip which increases manufacturing cost. The extra circuitry also increases power dissipation since every comparison circuit is active on every clock cycle. Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using a less costly method.

Fig 3 shows Generalised CAM structure of the size 16 word ,9 bit which will perform match operation in addition to read and write operation for any value of address and data bits .

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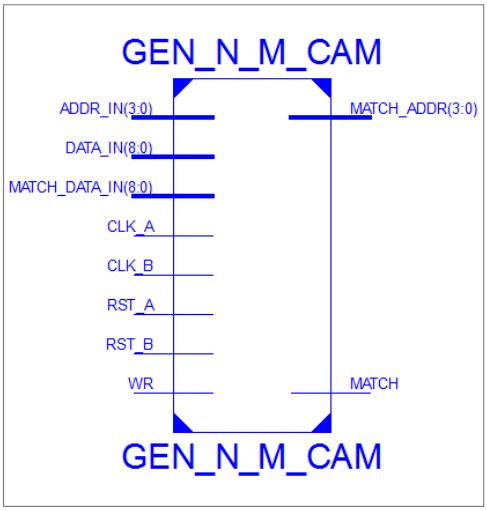
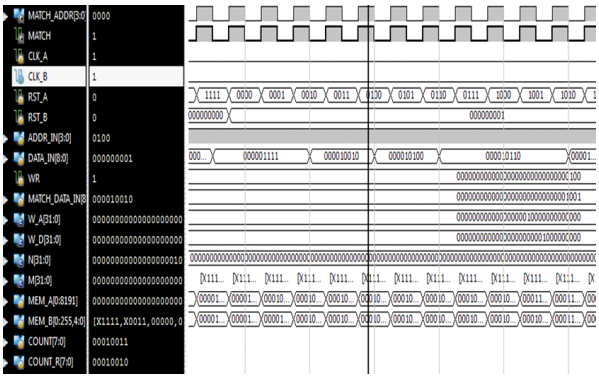
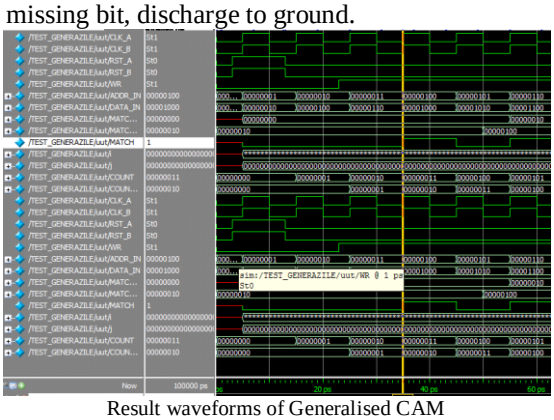


Fig 3 : Generalised CAM structure

Simulation Result : Thus content addressable memory compare input search data against stored data and return address of matched data indicating match signal bit high as shown in waveforms.



Here Input is associated with something stored in the memory.and Output is location where the associated content is stored.Thus CAM can be used as search engine. The search-data word is loaded into the search-data register. All match-lines are pre-charged to high (temporary match state). Search line drivers broadcast the search word onto the differential search lines. Each CAM core compares its stored bit against the bit on the corresponding search-lines.Match words that have at least one missing bit, discharge to ground.



Result waveforms of Generalised CAM

V. RESULT

Most memory devices store and retrieve data by addressing specific memory locations. As a result, this path often becomes the limiting factor for systems that rely on fast memory accesses. The time required to find an item stored in memory can be reduced considerably if the item can be identified for access by its content rather than by its address. A memory that is accessed in this way is called content-addressable memory or CAM. CAM can be used to accelerate any application requiring fast searches of data-base, lists, or patterns, such as in image or voice recognition, or computer and communication designs. For this reason, CAM is used in applications where search time is very critical and must be very short.

VI . CONCLUSION AND FUTURE SCOPE

For any application that requires a fast memory search, CAM can provide a solution. CAM can be used to accelerate any applications ranging from local-area networks, database management, file-storage management, pattern recognition, artificial intelligence, fully associative and processor-specific cache memories, and disk cache memories. Although CAM has many applications, it is particularly well suited to perform any kind of search operations. In the coming months, CAM will enjoy increased popularity, particularly with the growing number of communications applications that can utilize its capabilities.

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