IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 5, May 2018

Optimization of Half, Full and 4 Bit Ripple Carry Adders

Sandhya Bhardwaj[1], Anuj Sharma[2]

M.Tech Scholar, ECE Department, Sachdeva Institute of Technology, Mathura, India[1]

Assistant Professor, ECE Department, Sachdeva Institute of Technology, Mathura, India[2]

Abstract: In this paper, a varied range of adder circuits are designed in which half adder cmos, full adder cmos and RCA cmos are included, are designed using MOSFET in 32nm Technology length. Then, they are simulated using HSPICE and the performance parameters of adders such as average power and delay are determined. A dual mode low power technique is applied on Ripple Carry Adder to reduce power.

Keywords: Adder, Dual-Mode, 32nm.

1. INTRODUCTION

As nanometer process innovations have propelled, chip thickness and working recurrence have expanded, making power utilization in battery-worked versatile gadget. Notwithstanding for non-compact gadgets, control utilization is vital on account of the expanded bundling and cooling costs and also potential unwavering quality issues. [3]Along these lines, the principle outline objective for VLSI (extensive scale) architects is to meet execution necessities inside a power spending plan. In this manner, control effectiveness has expected expanded significance.[1] The desire to improve the plan measurements of execution, control, territory, cost, and time to advertise (opportunity cost) has not changed since the origin of the IC business. Truth be told, Moore's Law is tied in with streamlining those parameters.[6] Be that as it may, as scaling of assembling hubs advanced towards 20-nm, a portion of the gadget parameters couldn't be scaled any further, particularly the power supply voltage, the predominant factor in deciding dynamic power. What's more, enhancing for one factor, for example, execution consequently converted into enormous bargains in different zones, similar to control.[4] Another restriction as procedures moved toward 20-nm was the way that lithography was stuck at ArF brightening source with a wavelength of 193nm while the procedure basic element was pushing sub-20nm. Optical developments, for example, submersion lithography and twofold designing made that conceivable, yet at the cost of expanded inconstancy.

2. ADDER

The subsequent reenactments are ascertained on summation HSPICE by utilizing coding the hubs of the circuit outline, the circuit chart hubs are given extraordinary hub call, for which the MosFET variant from BSIM is covered and simulated. The 1 bit operation- bit code selects the result of the arithmetic block to be the output of the Adder.

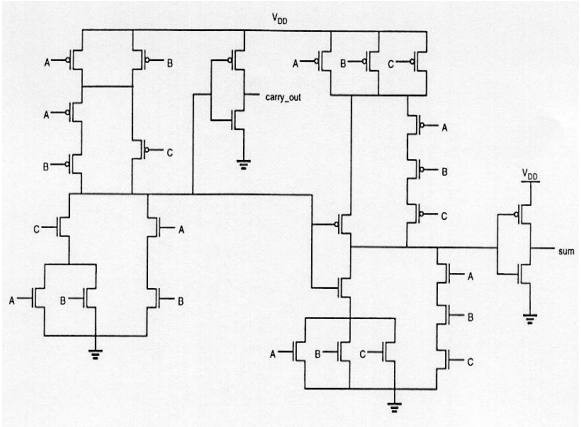

Figure 2: Full Adder Design Block Diagram for Transistor Level

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Figure 3 and 4 represent adder design for half adder and ripple carry adder and Figure 5 shows the dual mode representation.

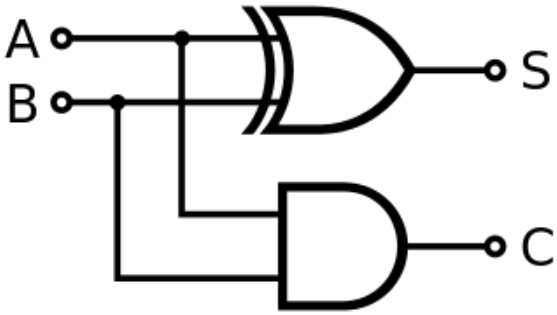

Figure 3: Half Adder Gate Level Block Design

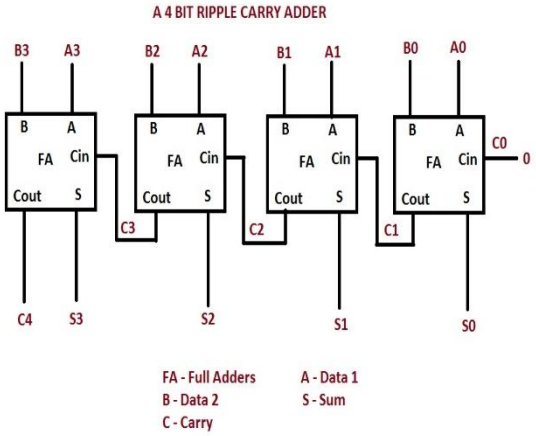

Figure 4: Ripple carry Adder

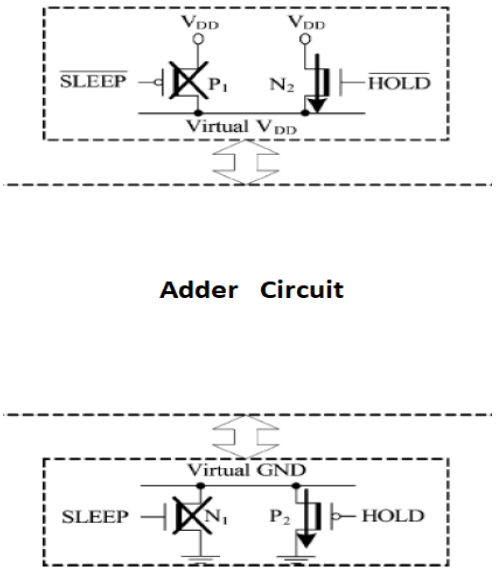

Figure 5: Dual Mode Technique Basic Block Diagram

Two modes are involved in dual mode technique, one is for hold mode and other is for sleep mode.

3. Simulation Results:

Results are obtained on synopsys HSPICE software and models of MosFET from PTM website, i.e. Predictive Technology Model**.** The Adder is implemented on 32nm Technology of MosFET using conventional CMOS technique and dual-mode technique.

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Results show that dual mode technique is more efficient in terms of average power consumption and delay. In figure 6, Average power comparison chart is shown for full adder, similarily in figure 7, for half adder. For ripple carry adder Figure 8 and 9 show charts for average power and delay.

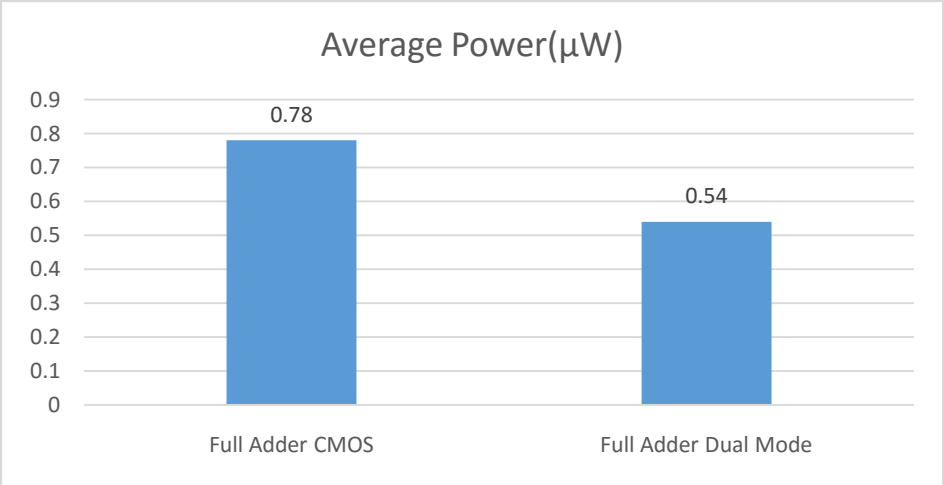

Figure 6: Average Power Full Adder

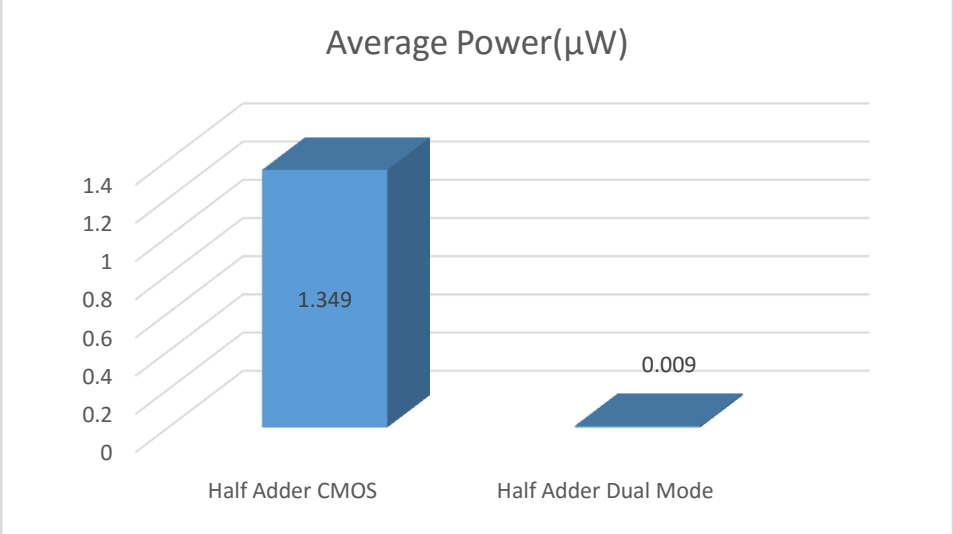

Figure 7: Average Power Half Adder

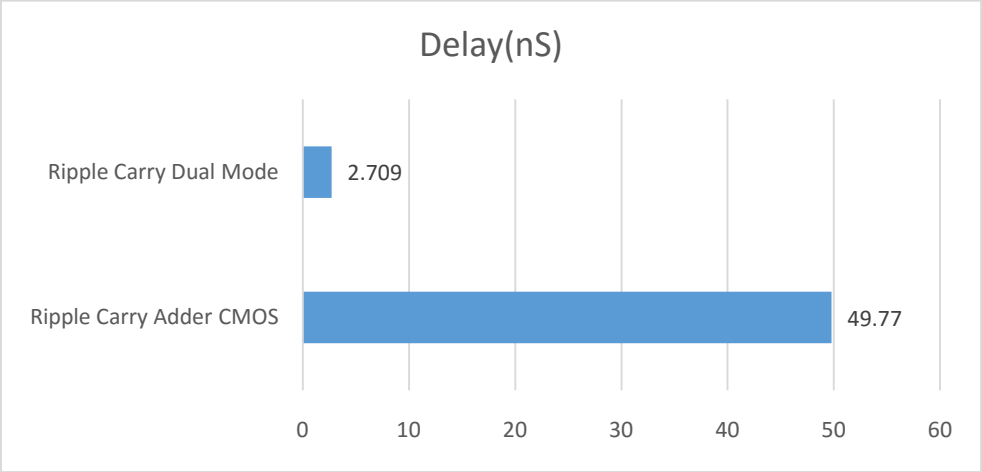

Figure 8: Delay for Ripple Carry Adder

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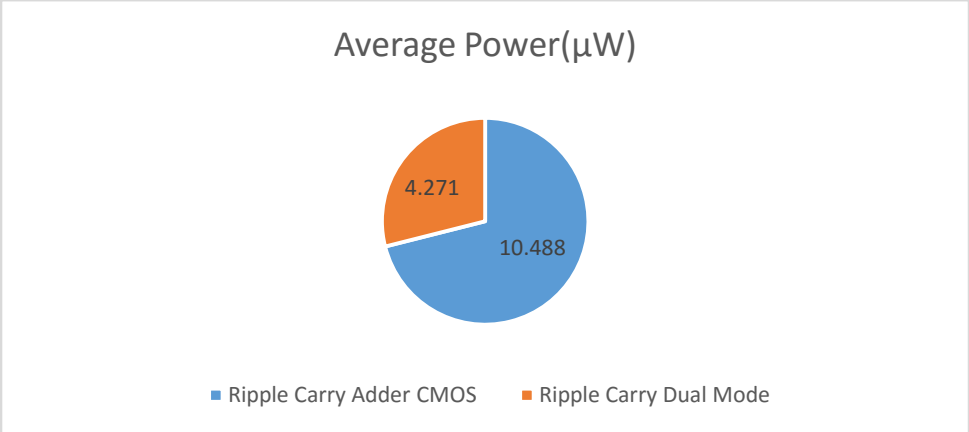

Figure 9: Average Power Pie chart for ripple carry adder

Table 1 represents comparison of both average power and delay for the designed adders.

Table 1: Data for Average Power and delay for designed Adder Circuits

	Half Adder CMOS	Half Adder Dual Mode
Average Power(µW)	1.349	0.009
	Full Adder CMOS	Full Adder Dual Mode
Average Power(µW)	0.78	0.54
	Ripple Carry Adder CMOS	Ripple Carry Dual Mode
Average Power(µW)	10.488	4.271
Delay(nS)	49.77	2.709

4. CONCLUSION

On the basis of simulation results obtained on HSPICE software, dual mode technique gives significant improvement in Average power consumption in all the adder cmos circuits, thereby increasing its performance of durability and efficiency of the cmos circuit. It is also observed that by adding two modes namely sleep and hold mode for the circuits, we get improvement in the speed of the circuit by reducing the delay. It is necessary step to improve the power consumption and speed as in present scenario more and more portability of electronics devices is required. With use of the proposed technique, in vlsi a significant improvement in efficiency can be obtained.

REFERENCES

[1] P. Balasubramanian, "Approximated Ripple convey adders and convey look forward adders-similar anaysis" IEEE , October 2017
[2]Sarabdeep Singh,Dilip Kumar, Design of Area and Power Efficient Modified Carry Select Adder,International Journal of Computer Applications,vol.33,no.3,pp.14-18,Nov2011.
[3] www.circuitstoday.com/swell pass on adder
[4] Carry look forward adder Hardware estimations for math modules, ARITH investigate gathering, Aoki lab., Tohoku University
[5] International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 10, October 2014 Copyright to IJARCCE www.ijarcce.com 8341 Implementation of Ripple Carry and Carry Skip Adders with Speed and Area Efficient PUSHPALATHA CHOPPA, B.N. SRINIVASA RAO
[6] www.barrywatson.se/dd/dd_Carry _select_adder.html
[8]tams-www.informatik.uni-hamburg. de/applets/hades/webdemos/20-number juggling/65-csa-mult/csa6.html
[9] Arkadiy Morgenshtein, Alexander Fish and Israel A.Wagner "Entryway Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits ", IEEE exchanges on VLSI Systems, vol.10, no. 5 , pp.566-581, October 2002.
[10] Moradi, F. Wisland, D.T. Mahmoodi, H. Aunet, Tuan Vu Cao and Peiravi "Ultra low power full adder topologies", in: Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS, pp. 3158, 3161, May 2009.
[11] Po-Ming Lee, Chia-Hao Hsu and Yun-Hsiun Hung, "Novel 10-T full adders acknowledged by GDI structure",in: Proceedings of IEEE International Symposium on Integrated Circuits (lSIC), pp.115,118, Sept. 2007.
[12] Q. Wu, P. Massoud, X.Yu, "Clock-Gating and Its Application to Low Power Design of Sequential Circuits," in Proceedings of the IEEE Conference on Custom Integrated Circuits, pp. 425-435, September 1997.
[13] Padmanabhan Balasubramanian and Johince John "Low Power Digital outline utilizing changed GDI strategy", in: Proceedings of International Conference on Design and Test of Integrated Systems in Nanoscale Technology, DTIS, pp.190,193, Sept. 2006.
[14] Dubey, V. Sairam, R., "An Arithmetic and Logic Unit Optimized for Area and Power", in: Proceedings of International Conference on Advanced Computing and Communication Technologies (ACCT), pp.330, 334, Feb. 2014.
[15] Manjunatha Reddy, B.N. Sheshagiri, H.N. Vijayakumar and B.R. Shanthala, "Execution of Low Power 8-Bit Multiplier Using Gate Diffusion Input Logic", in: Proceedings of IEEE seventeenth International Conference on Computational Science and Engineering (CSE), pp.1868, 1871, Dec. 2014.
[16] Alireza Saberkari and Shahriar Baradaran Shokouhi, "A novel low-control low-voltage CMOS 1-bit full adder cell with the GDI method", in: Proceedings of the IJME-INTERTECH Conference, pp. 758,765, August 2006.