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An Optimized XOR Circuit using CNTFET Technology

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Abstract: In this paper, a varied range of XOR circuits are designed in which 6T XOR is proposed using CNTFET Technology are designed using MOSFET in 32nm Technology length. Then, they are simulated using HSPICE and the performance parameters of adders such as average power and delay are determined. The proposed circuit is compared with 12T CMOS XOR circuit which is conventional used and compared with CNTFET counterpart of the XOR gate. Simulation results show that the proposed XOR gate is better in performance.

Keywords: CNTFET, Nano tubes, XOR, 32nm, 6T XOR.

1. INTRODUCTION

In a MOSFET, the source and deplete are associated by a leading surface channel through which bearers can stream when legitimately regulated by the door voltage [1]. The source and deplete areas can be either p or n write, yet they should both be of a similar sort, and of inverse kind to the body district. As of late, MOSFETs have been downsized fundamentally and the Si-SiO2 interface remains the most critical mix [2]. Downsizing the measurements of MOSFETs is a constant pattern. The challenges with diminishing the extent of the MOSFET incorporate the semiconductor gadget manufacture process, the requirement for low voltages, and with poorer electrical execution the need of circuit upgrade and advancement [3]. It has been expressed that littler transistors switch quicker, which is the primary inspiration for downsizing the measurements of semiconductor gadgets [4]. Carbon nanotubes, as novel materials with one of a kind electronic qualities, have been expected to be abused to build electronic gadgets for their preferable physical properties over those of conventional used silicon, for instance, longer mean freeway, bigger transporter versatility, and higher transport current thickness. [8] This area presents the attributes of carbon nanotubes and portrays a portion of their potential applications. In the light of transport conductivity, carbon nanotubes can be catalogued as metallic or semiconducting carbon nanotubes [5], which is decided by the energy band gap between the atoms. The conductive type of the CNTs depends on its chirality [6]. Both metallic and semiconducting CNTs have been studied as potential electronic components and their electronic properties have been established.[11]

2. CNTFET TECHNOLOGY

The activity standard of Carbon Nanotube Field-Impact Transistor (CNFET) is like that of conventional silicon gadgets. This three (or four) terminal gadget comprises of a semiconducting nanotube, going about as leading channel, connecting the source and deplete contacts. The gadget is turned on or off electro statically by means of the door. The semi 1D gadget structure gives better door electrostatic control over the channel district than 3D gadget (e.g. mass CMOS) and 2D gadget structures [10]. As far as the gadget task instrument, CNFET can be classified as either Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET-like FET[3][4][12]. The conductivity of SB-CNFET is represented by the larger part bearers burrowing through the SBs toward the end contacts. [12]The on-current and subsequently gadget execution of SB-CNFET is controlled by the contact protection because of the nearness of burrowing boundaries at both or one of the source and deplete contacts, rather than the channel conductance, as appeared by Fig 1.3(a). [14]The SBs at source/deplete contacts are because of the Fermi level arrangement at the metal-semiconductor interface.[15][9] Both the stature and the width of the SBs, and along these lines the conductivity, are adjusted by the entryway electrostatically. SB-CNFET indicates ambipolar transport conduct [4]. Figure 1 and 2 show energy band diagram of CNTFET in SB and MOS like form and an ideal cntfet representation.

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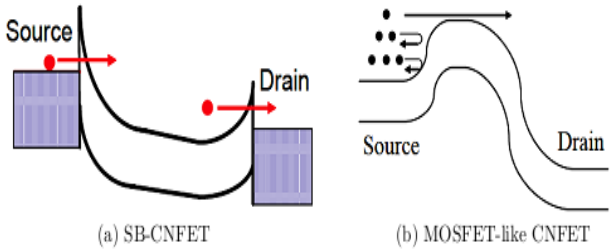

Figure 1: Band diagram for Energy(a) Schottky Barrier-CNFET and (b) MOS-like CNFET.

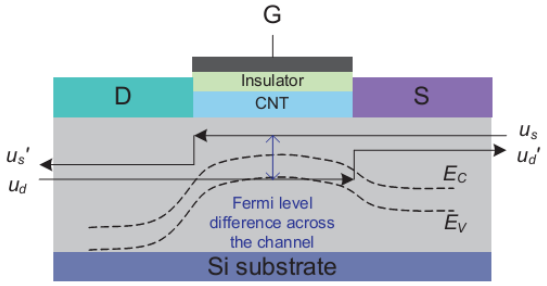

Figure 2: Ideal CNTFET

3. PROPOSED XOR DESIGN USING CNTFET

In hardware, a XOR is a circuit that duplicates two stable states and is utilized as a fundamental piece in an Arithmetic and Logic Unit. It is imperative to enhance parameters in a XOR as it most ordinarily utilized piece of rationale unit. In our proposed strategy, we supplant regular MOSFETs with CNTFETs, and a comparitive examination of measurements like Average Power Consumption, Delay, PDP and Power Dissipation Voltage Source is computed.It is found that in terms of all performance metrics mentioned, the 6T CNTFET circuit is the best configuration circuit for XOR gates.

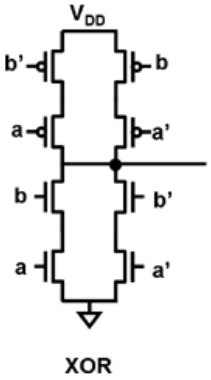

Figure 3: 12T CMOS XOR Gate

The proposed design of 6T XOR is given in Figure 4 and in Figure 3 Conventionally used 12T XOR gate is shown. In 6T XOR, basically two inverters and one pass transistor forms the logic of XOR gate. As in XOR gate, when both inputs are different output is 1 and when both inputs are same output is 0. This can be easily verified on the 6T XOR gate.

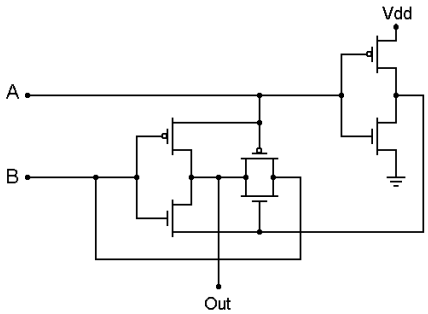

Figure 4: Circuit for 6T XOR using MOSFET

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While using CNTFET, we have to consider several factors like no. of tubes, pitch, width efeective, etc, the schematic is similar to the MOSFET one by changing the device to CNTFET as shown in Figure 5 and Figure 6. In Figure 5, circuit of conventional XOR gate 12T using CNTFET is shown. And in Figure 6, circuit of proposed CNTFET based 6T XOR gate is shown.

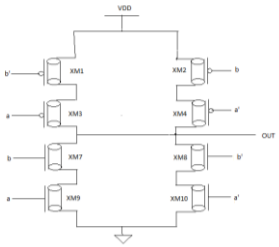

Figure 5: Circuit for 12T XOR usingCNTFET

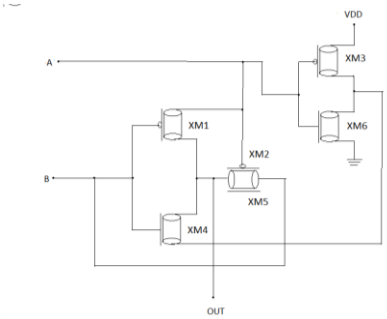

Figure 6: Proposed Circuit for 6T XOR usingCNTFET

Our proposed method for making a XOR functianlity utilizing CNFET working precisely and the outcomes are exhibited out in this paper. For the reenactment we utilize the stanford CNFET Hspice demonstrate for Simulation at 32nm innovation. The proposed technique improves the transistor circuit Average Power Consumption, Delay, PDP and Power Dissipation Voltage Source Parameters.

4. SIMULATION RESULTS

This has been proficient by proposing another enhancement strategy. To demonstrate the adequacy of the proposed gate level plan technique, recreation has been performed utilizing HSPICE with the Stanford CNTFET library. [13]Results have shown that the proposed outline approach is both successful and common. To outline a CNTFET circuit, numerous parameters must be considered, among them the distance across at certain chirality, pitch. The parameters, for example, limit voltage, gate capacitance, deplete present, ideal fan-out factor can be controlled by pitch, chirality and the quantity of carbon nano tubes. Table 1 introduces the measurements correlation between CNTFET based XOR and MOSFET based XOR.

Figure 7 and Figure 8 shows to Average Power Comparison in XOR 12T and 6T. It obviously demonstrates that CNTFET XOR in 32nm innovation is a superior choice with 6T. In table 1 all simulation results are presented,

Table 1: Simulation Results

	12T XOR MosFET	12T XOR CNTFET
Average Power (12T)	6.50E-07	3.57E-07
Delay (12T)	4.76E-08	4.79E-08
PDP	3.09E-14	1.71E-14
	6T XOR MosFET	6T XOR CNTFET(proposed)
Average Power (6T)	1.95E-06	7.26E-08
Delay (6T)	8.96E-11	8.81E-11
PDP	1.75E-16	6.40E-18

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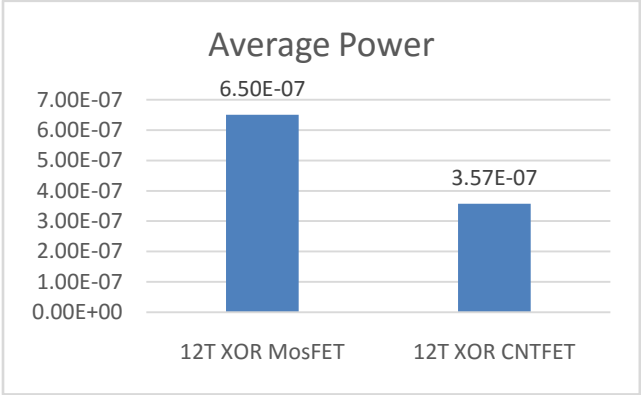

Figure 7: Average Power in XOR 12T

In Figure 9 Delay comparison of 6T XOR is represented. Table 1 gives a tabular representation of the results.

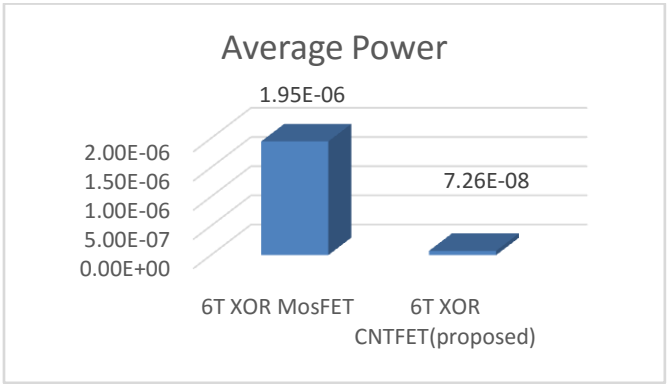

Figure 8: Average Power in XOR 6T

It shows when we use CNTFET replacements the Delay, Average Power Consumption, PDP and Power Dissipation for Voltage a significant improvement in all is obtained in XOR 6T and XOR 12T circuits.

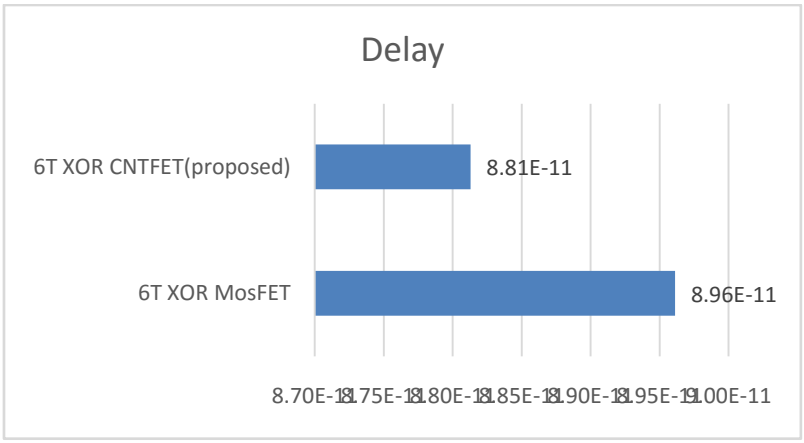

Figure 9: Delay in XOR 6T

Figure 11 and Figure 12 are charts which represent that PDP is improved when using CNTFET and comparing to MOSFET based XOR in 6T and 12T modes.

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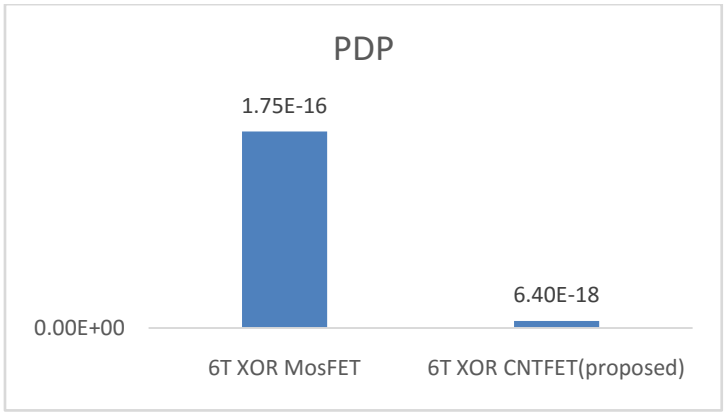

Figure 11: PDP in XOR 6T

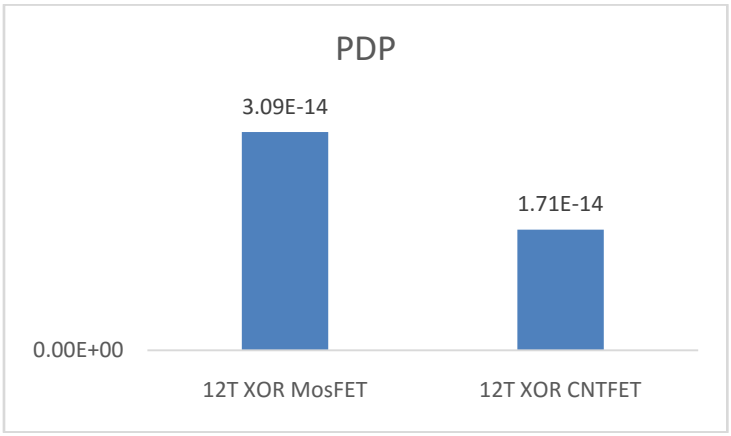

Figure 12: PDP in XOR 12T

Above results show that CNTFET is the device which can be used to replace MOS type circuits at lower scaled technologies.

CONCLUSION

Simulation results show that 6T CNTFET is better in case of XOR gates as Average Power is reduced by 79% and Delay is also reduced by 99.8%. Also significant improvement in the PDP and 72.9 % when compared to 12TXOR gate. The Carbon Nanotube Field Effect Transistor (CNTFET) is a standout amongst the most encouraging gadgets among rising advancements to broaden as well as supplement the conventional Si MOSFET. As the qualities of a CNTFET is not the same as traditional mass CMOS, new plan technique must be built up. As request of new outline technique, this task break down the qualities of CNFET, CNT interconnect advances and propose new strategies to configuration circuits, for example, computerized, memory and I/O circuit. To demonstrate the viability of the proposed entryway level plan technique, reproduction has been performed utilizing HSPICE with the Stanford CNTFET library. Results have exhibited that the proposed outline system is both successful and functional.

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