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Analysis of Low Power and High Speed Double Tail Comparator using FinFET Technology

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Abstract: In conventional double tail comparators, Kick-back noise is produced and the circuit requires high input impedance. Due to aggressive scaling of MOS, short channel effects occur and there is a need of substitutes like FinFETS. In this paper, we have designed double tail comparator by using FinFET technology in shorted gate mode. It is seen from results that the power and delay are reduced in a large quantity maintaining the output waveforms to the previous one. This improves efficiency of the system and noise tolerance and leakage current are also reduced. This can be beneficial for the Analog to Digital Converters, reference voltage comparison.

Keywords: FinFET, Double tail Comparator, 32nm, MOSFET

1. INTRODUCTION

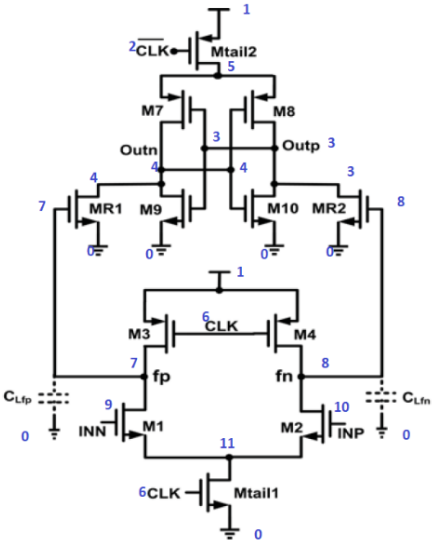

Figure 1: Conventional double tail comparator

In figure 1 conventional double tail comparator is shown. This is also implemented using FinFET Technology to check feasibility of the circuit. The working of the double tail comparator is explained below.

1.1 Operation of Double Tail Comparator: The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption [1],[5] is shown in Fig. 1. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. Figure 2 shows proposed circuit of FinFET technology double tail comparator. In this 4 transistors are added and two signals fn and fb for stacking which reduces power consumption. But in 32nm, short channel effects prevent further improvement; this motivates to change the transistor technology.

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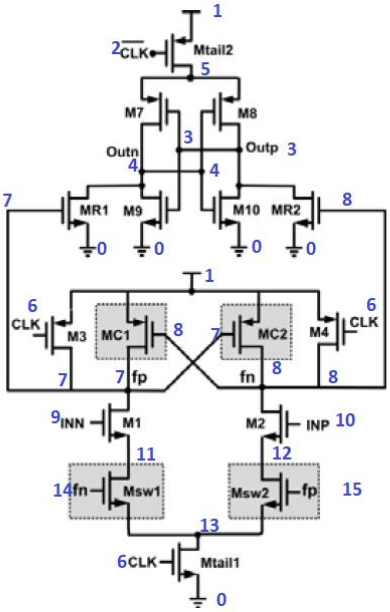

Figure 2: Proposed circuit using FinFET

Due to the better performance of double-tail architecture in low-voltage applications [2], the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed [4]. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

The operation of the proposed comparator is as follows:

During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor trans-conductance and input voltage difference in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time . Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

2. SIMULATION RESULTS

The simulations are performed on HSPICE Software, BSIM CMG FinFET Model is used and PTM BSIM MOSFET in 32nm technology. The output waveform of double tail comparator is shown in Figure 3 below. The signal 2 and 6 are clock bar and clock, 9 and 10 are inputs, and 3 and 4 are outputs of the comparator. It is seen that by using FInFET technology same output can be achieved with lower consumption and propagation delay.

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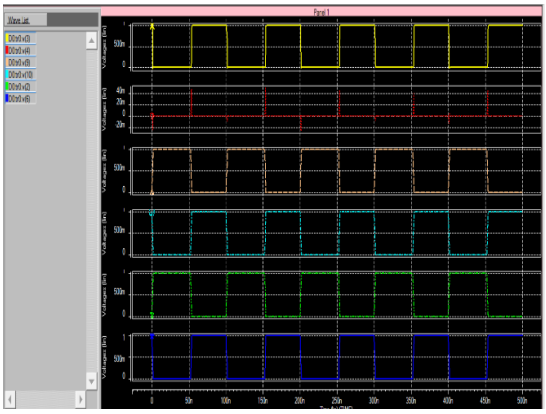

Figure 3: Output Waveform of Comparator

2.1 Average Power & Delay Calculations: Figure 4 and Figure 5 shows average power results of MOSFET and FinFET based double tail comparator in conventional and proposed devices for double tail comparator.

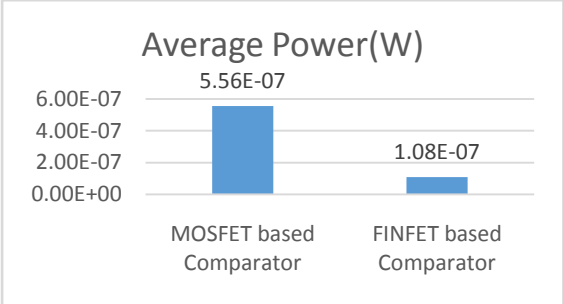

Figure 4: Average Power Comparison Conventional

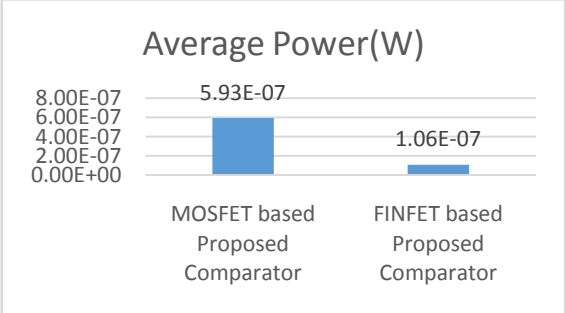

Figure 5: Average Power Comparison Proposed

Figure 6 and Figure 7 shows delay results of MOSFET and FinFET based double tail comparator in conventional and proposed devices for double tail comparator.

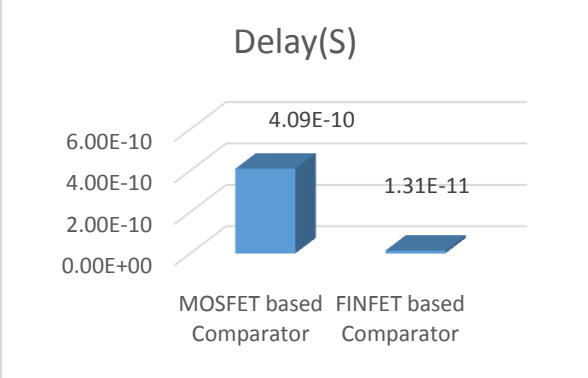

Figure 6: Delay Comparison Conventional

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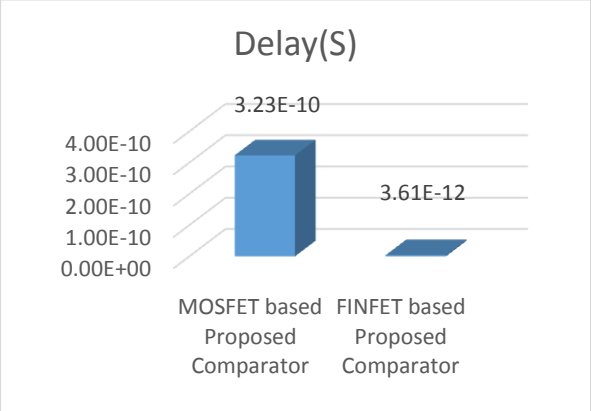

Figure 7: Delay Comparison Conventional Proposed

Table 1 and Table 2 shows average power and delay results of MOSFET and FinFET based double tail comparator in conventional and proposed devices for double tail comparator.

Table 1: Results of Conventional Comparator

circuit1	MOSFET based Comparator	FINFET based Comparator
Average Power(W)	5.56E-07	1.08E-07
Delay(S)	4.09E-10	1.31E-11

Table 2: Results of Proposed Comparator

circuit2	MOSFET based Proposed Comparator	FINFET based Proposed Comparator
Average Power(W)	5.93E-07	1.06E-07
Delay(S)	3.23E-10	3.61E-12

CONCLUSION

Simulation results show that DOUBLE TAIL COMPARATOR conventional and proposed have improved speed and a lower consumption of average power. The average power and delay is improved by 80.5 % and 96.7% respectively for conventional DOUBLE TAIL COMPARATOR MOSFET and FinFET. For proposed DOUBLE TAIL COMPARATOR, the FinFET DOUBLE TAIL COMPARATOR is improved by 82.12% in Average Power and in Delay it is improved by 98.8%.

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