ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 7, Issue 8, August 2018

Optimization of Low Power CMOS based Voltage Reference Generator in 32nm

Sneha Meshram[1], Uday Panwar[2]

Student, Dept. of Electronics and Communications, Sagar Institute of Research and Technology, Bhopal, India[1]

Associate Professor, Dept. of Electronics and Communications,

Sagar Institute of Research and Technology, Bhopal, India[2]

Abstract: In this paper, a CMOS based low power voltage reference generator is optimized in 32nm technology. Circuit's temperature dependencies and threshold voltage dependencies is studied and improved to give higher reference voltage generated in low power applications. The simulation are performed on Synopsys HSPICE software. Simulation results shows higher reference voltage is obtained with low power consideration and under different temperatures giving minimal variations over temperatures in the voltage reference output.

Keywords: Voltage Reference, 32nm MOSFET, Analog Circuit, 32nm FinFET

1. INTRODUCTION

A coordinated voltage reference has turned into a fundamental piece of relatively every IC. Voltage references are required for Analog to Digital Converters (ADC's) and voltage controllers. Incorporating the voltage reference has the advantage of lessening the cost for the end client. In this segment, standard reference voltage configuration will be depicted. Normal reference voltages depend on the bandgap voltage of silicon. A bandgap reference circuit includes a base-producer voltage with negative temperature coefficient with a scaled adaptation of the warm voltage to accomplish a temperature autonomous voltage that is identified with the bandgap of silicon.

While talking about the plan of a low commotion CMOS voltage reference, it is important to investigate the general execution constraints of voltage references to better comprehend the upsides of building such a circuit. The undeniable reason for any voltage reference is to give a steady estimation of voltage over a given scope of working conditions. A real circuit's execution will be obliged by its total mistake (how shut the yield voltage can be set to a coveted an incentive at ostensible working conditions) and its relative blunder (how much the voltage fluctuates from the ostensible incentive over the full scope of working conditions). Since elite voltage references by and large have a few methods for trimming their ostensible yield esteem [4], [5], the total blunder can successfully be set to zero by altering the circuit. In these cases, relative blunder will decide the cutoff of the voltage reference's convenience. On the off chance that a top notch voltage reference is required which can be coordinated into a mass CMOS process without the utilization of outer segments, the best circuit decision is the bandgap reference. Bandgap references are effortlessly actualized in CMOS, along these lines it is vital to consider the impacts of limit voltage and temperature utilizing a reasonable examination set as performed in this exploration. Coming about because of the across the board utilization of compact gadgets, the improvement of voltage reference with little region, low supply voltage, low power and superior, broadly utilized as a part of simple and blended mode circuit, for example, A/D and D/A converters, DC– DC converters, PLLs and others are advanced. Voltage reference produces a DC voltage autonomous of temperature, supply voltage and creation process [1]. Conventional voltage reference depends on the silicon bandgap voltage, which is approximately1.2Vand limits the base supply voltage of the whole circuit. Also, bandgap voltage circuit is infeasible for process without bipolar. This paper is organized as follows, in section 1 a brief introduction is given on Voltage Reference Generators CMOS based, Section 2 gives implementation and simulation of the circuit based CMOS body bias technique as presented in [1]. While section 3 is conclusion and then references are mentioned.

2. IMPLEMENTATION AND SIMULATION RESULTS

The circuit under consideration is shown in Figure 1. This is a voltage reference generator based on CMOS using body-bias technique. This circuit is divided into three parts: the start-up circuit, current source and the output circuit. The start-up circuit provides the initialization of the circuit and current source produces a current independent of voltage supply and output part produces a reference voltage. This circuit is also implemented using FinFET Technology for DGFETs (Double Gate Field Effect Transistors). In these two configurations, a comparative analysis is prepared on the basis of few performance metrics like Average Power, Reference Voltage, Delay and PDP.

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 7, Issue 8, August 2018

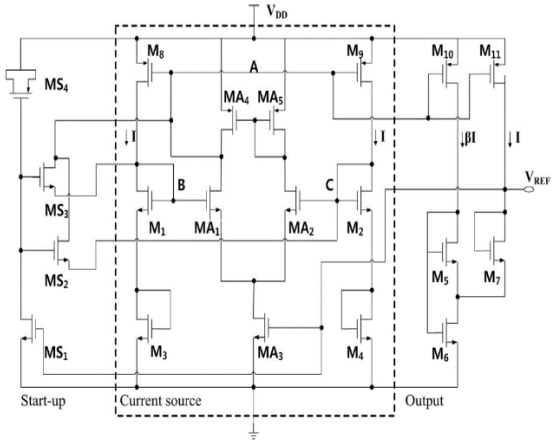

Figure 1: Schematic of Voltage Reference Generator [1]

Also Monte Carlo Simulation is performed by varying threshold voltages of the transistors. A transient analysis by varying temperature of operation is also performed.

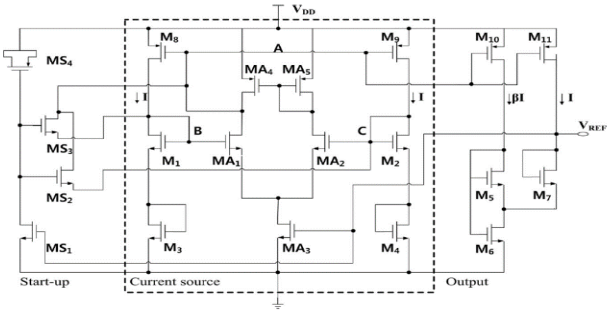

Figure 2: Realization Of Voltage Reference Generator using MOSFET

The simulated output of Voltage Reference Generator CMOS is shown in figure 4.3

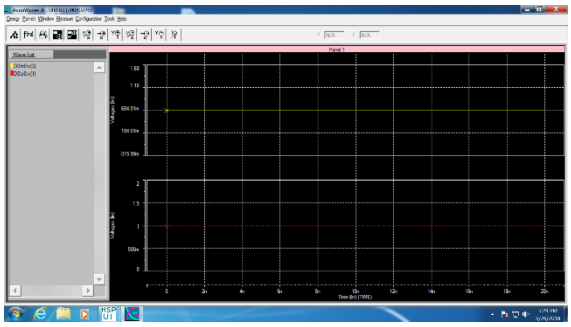

Figure 3: Waveforms of Voltage Reference Generator using MOSFET

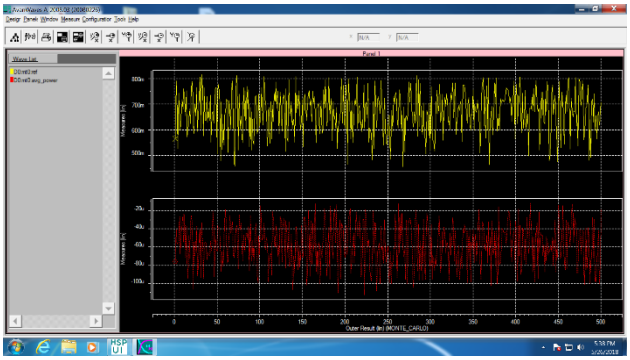

Figure 4: Waveforms of Monte Carlo Simulation on varying threshold voltage using MOSFET

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 7, Issue 8, August 2018

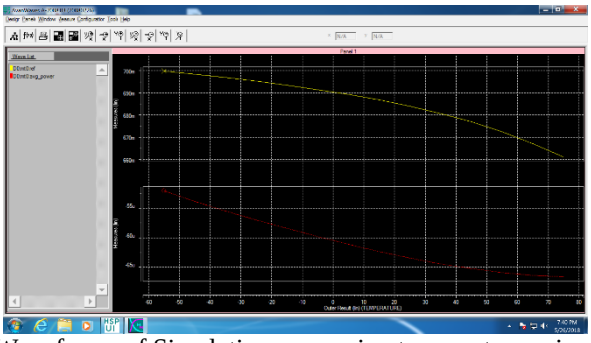

Figure 5: Waveforms of Simulation on varying temperature using MOSFET

4.2 Implementation of Voltage Reference Generator using FinFET in 32nm Technology:

The Voltage Reference Generator is realized using FinFETS as shown in figure 4.5:

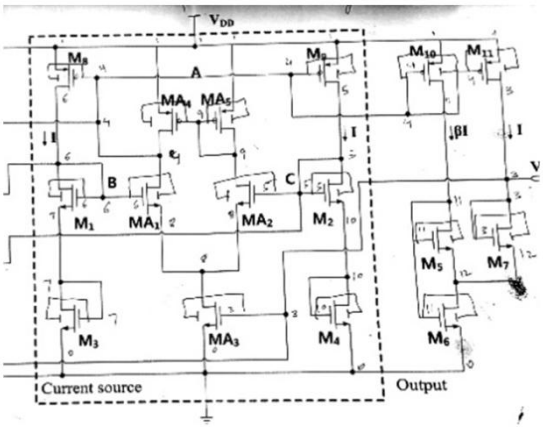

Figure 6: Realization of Voltage Reference Generator using FinFET

The simulated output of Voltage Reference Generator using FinFET is shown in figure 4.6

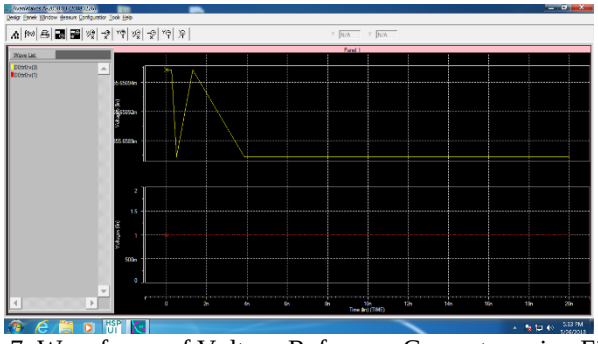

Figure 7: Waveforms of Voltage Reference Generator using FinFET

It is obvious that in FinFET higher voltage reference is generated than in mosfet counterpart.

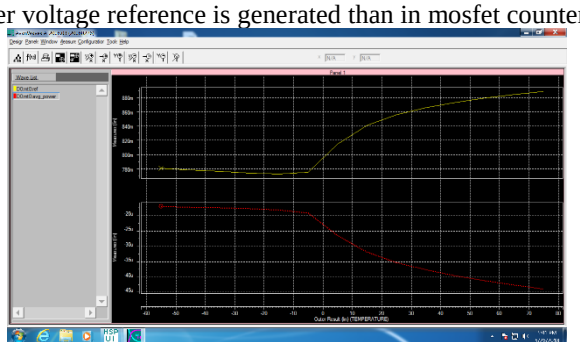

Figure 8: Waveforms of Simulation on varying temperature using FinFET

DOI 10.17148/IJARCCE.2018.7810

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 7, Issue 8, August 2018

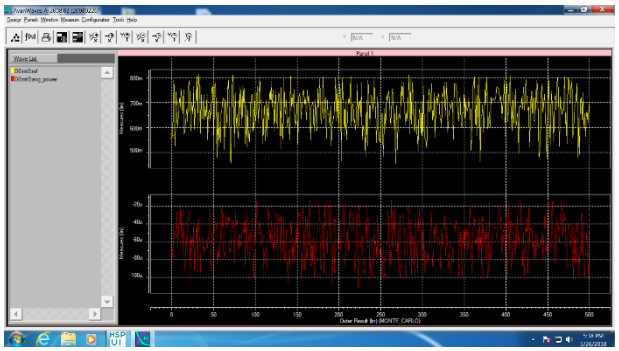

Figure 9: Waveforms of Monte Carlo Simulation on varying threshold voltage using FinFET

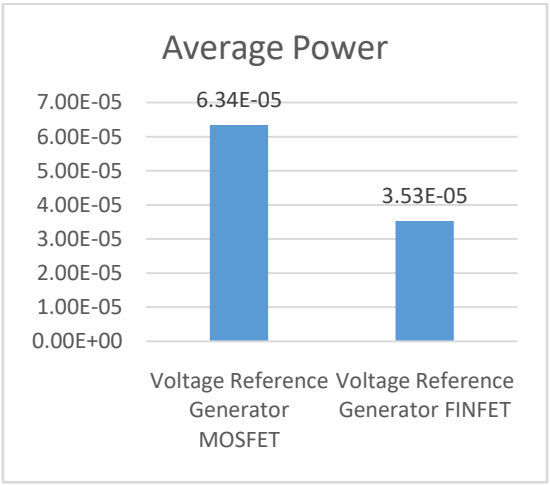

Figure 10: Average Power for Voltage Reference Generator

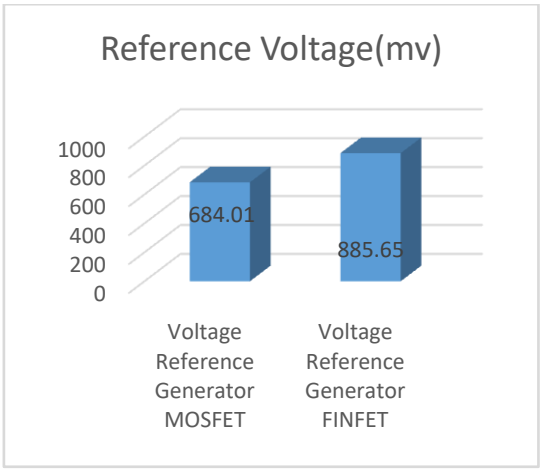

Figure 11: Voltage Reference Comparison

Table 5.1 represents comparison of both average power and reference voltage for the designed Voltage Reference Generators.

Table 1: Data for Average Power and Reference Voltage for designed Circuits

	Voltage Reference Generator MOSFET	Voltage Reference Generator FINFET
Average Power	6.34E-05	3.53E-05
	Voltage Reference Generator MOSFET	Voltage Reference Generator FINFET
Reference voltage(mv)	684.01	885.65

DOI 10.17148/IJARCCE.2018.7810

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 7, Issue 8, August 2018

3. CONCLUSION

The Proposed CMOS Reference Circuit has been composed in standard 32 nm CMOS process that shows reference supply and temperature independency. The plan of CMOS Voltage Generator is by just subtracting two current yields with similar conditions on the supply voltage and temperature. While for Voltage Generator we utilized the Active load, which gives the fix estimation of voltage with varieties in supply voltage and temperature. Accomplished outcomes demonstrate that created Architecture of consolidated reference can be effectively utilized for oscillators and numerous other blended flag coordinated circuits.

REFERENCES

[1]. Yanhan Zeng n, Yirong Huang,Yunling Luo, Hong-Zhou Tan, “An ultra-low-power CMOS voltage reference generator based on body bias technique”, Elsevier, 0026-2692/$-seefrontmatter&2013Elsevier Ltd. All rights reserved. http://dx.doi.org/10.1016/j.mejo.2013.07.003.
[2]. G. A. Rincón-Mora, Voltage References – From Diodes to Precision High-Order Bandgap Circuits, IEEE Press, John Wiley and Sons, Inc., 2002, ISBN: 0471143367.
[3]. B. S. Melody and P. R. Dark, "An exactness bend remunerated CMOS bandgap reference," IEEE J. Strong State Circuits, vol. SC-18, pp. 634–643, Dec. 1983
[4]. Jiang Y, Lee E K F Design of low-voltage bandgap reference utilizing transimpedance intensifier. IEEE Transaction on Circuits and Systems 11,2000,47(6);552-555
[5]. H. Banba, H. Shiga, A. Umezawa, T. Miyabata, T. Tanzawa, S. Atsumi,and K. Sakuii, "A CMOS bandgap reference circuit with sub-1-V operation, "IEEE J. Strong State Circuits, vol. 34, pp. 670– 674, May 1999.
[6]. P. Maloberti, F. Fiocchi, C. Pruzzi, Curvature-remunerated BiCMOS bandgap with 1-V supply voltage. IEEE J. Strong State Circuits, 2001, Vol. 36(7):1076 - 1081
[7]. K. N. Leung and P. K. T. Mok, "A sub-1-V 15 ppm/°C CMOS bandgap voltage reference without requiring low limit voltage gadget," IEEE J. Strong State Circuits, vol. 37, pp. 526-530, Apr. 2002.
[8]. G. De Vita and G. Iannaccone, "A Sub-1-V, 10ppm/°C, Nanopower Voltage Reference Generator," IEEE J. Strong State Circuits, pp. 1536-1542, July 2007.
[9]. E. A. Vittoz and J. Fellrath, "CMOS simple incorporated circuits in light of powerless reversal task," IEEE J. Strong State Circuits, vol. SC-12, pp.224– 231, June 1977.
[10]. G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutr`ı, "A low voltage low-control voltage reference in light of sub-threshold MOSFETs," IEEE J. Strong State Circuits, vol.38, no.1,pp.151– 154, Jan.2003.
[11]. B.- S. Melody and P. R. Dim, "Edge voltage temperature float in particle embedded MOS transistors," IEEE J. Strong State Circuits, vol. SC-17,no. 2, pp. 291– 298, Apr. 1982.
[12]. Hong-Wei Huang, Chun-Yu Hsieh , Ke-Horng Chen , Sy-Yen Kuo, "A 1V 16.9ppm/°C250nA Switched-Capacitor CMOS Voltage Reference," ISSCC 2008/SESSION 24/ANALOG POWER TECHNIQUES/24.3
[13]. Yean-Kuo Luo, Ke-Horng Chen, Wei-Chou Hsu, "A double stage accuse direct controller of nano-ampere exchanged capacitor CMOS voltage reference for accomplishing low yield swells," the fifteenth IEEE International Conference on Electronics, Circuits and Systems, pp. 446 – 449, Sept. 3 2008