IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 8, Issue 6, June 2019

A 16X16 High Speed Vedic Multiplier for Area and Power Reduction

Mr.T.Muruganantham[1], Mr.N.R.Nagarajan[2], Mr.S.Syed Husain[3]

Assistant Professor, ECE, K.Ramakrishnan College of Engineering, Samayapuram, Trichy[1,2,3]

Abstract: This paper is motivated for the efficient high speed Vedic multiplier with implementation in FPGA. Recent and advanced Vedic multiplications of multipliers are implemented by using Urdhva tiryakbhyam multiplication technique is commonly used in different multiplier architectures. This multiplication algorithm is giving less delay and efficient power utilization with reduction of area. The 16x16 Vedic multiplier is synthesized in Xilinx and implemented in FPGA.

Keywords: Field Programmable Gate Array (FPGA), Vedic multiplier Technology

I. INTRODUCTION

The Vedic multiplier is working based on the methodology of Vedic multiplication. This multiplication method have been used to multiply ay two decimal numbers. In this paper we use the same methodology to the binary number system and to make the proposed compatible algorithm with hardware implementation. The Vedic multiplication is based on the Urdhva Triyakbhyam method. Urdhva Tiryakbhyam method is useful for different cases of multiplication. The algorithm can be used for n x n bits. The sums and products are executed in parallel and it is independent of clock of the processor, Due to this the multiplier requires reduced time and independency of clock frequency which reducing the power utilization. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of area and speed.

II.RTL SCHEMATIC OF VEDIC MULTIPLIER

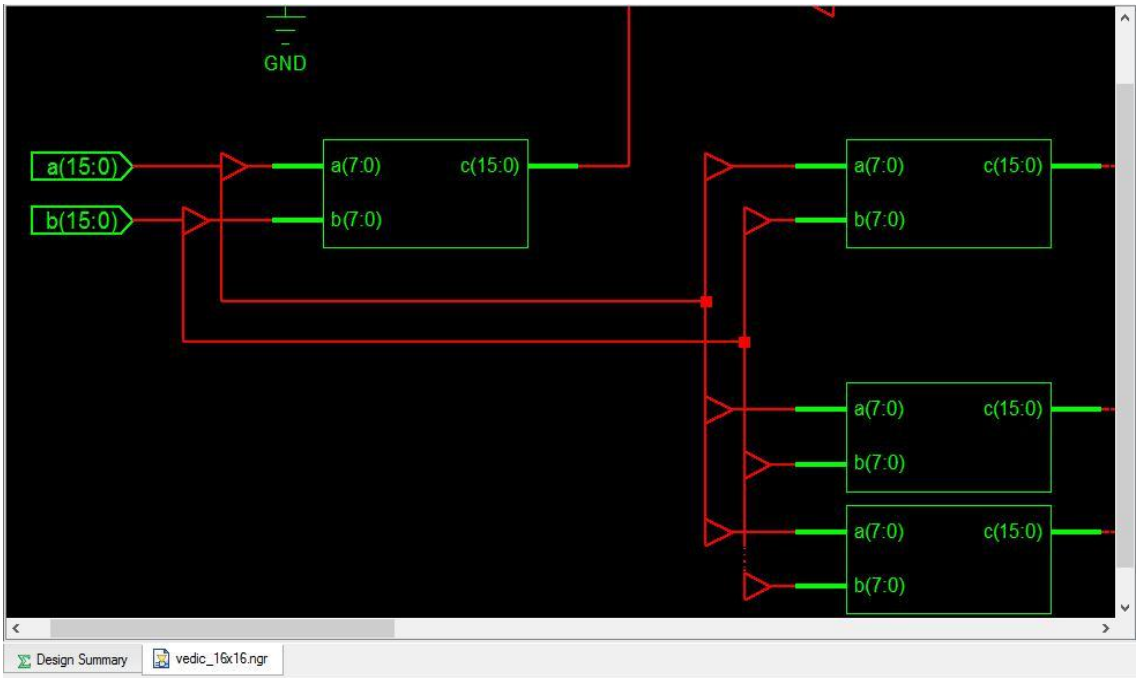

Fig.1.RTL Schematic of 16x16 Vedic Multiplier Technology

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 8, Issue 6, June 2019

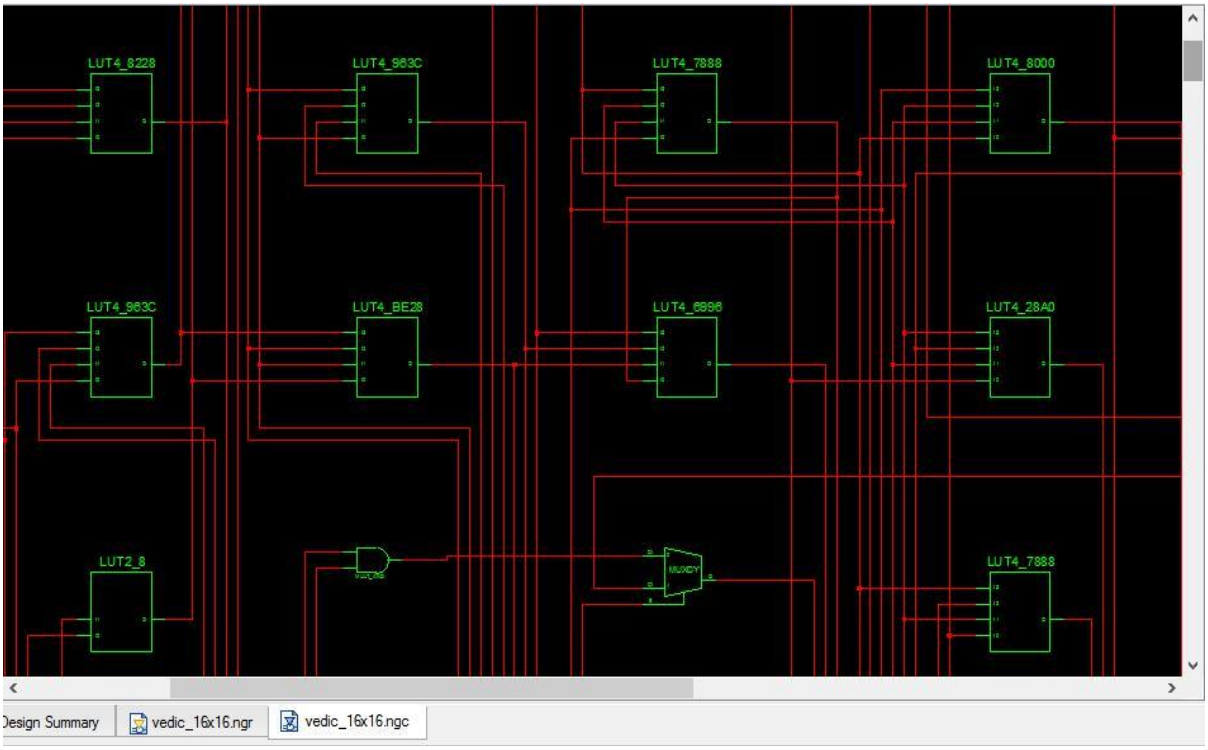

Fig2.Technology Schematic of 16x16 Vedic Multiplier

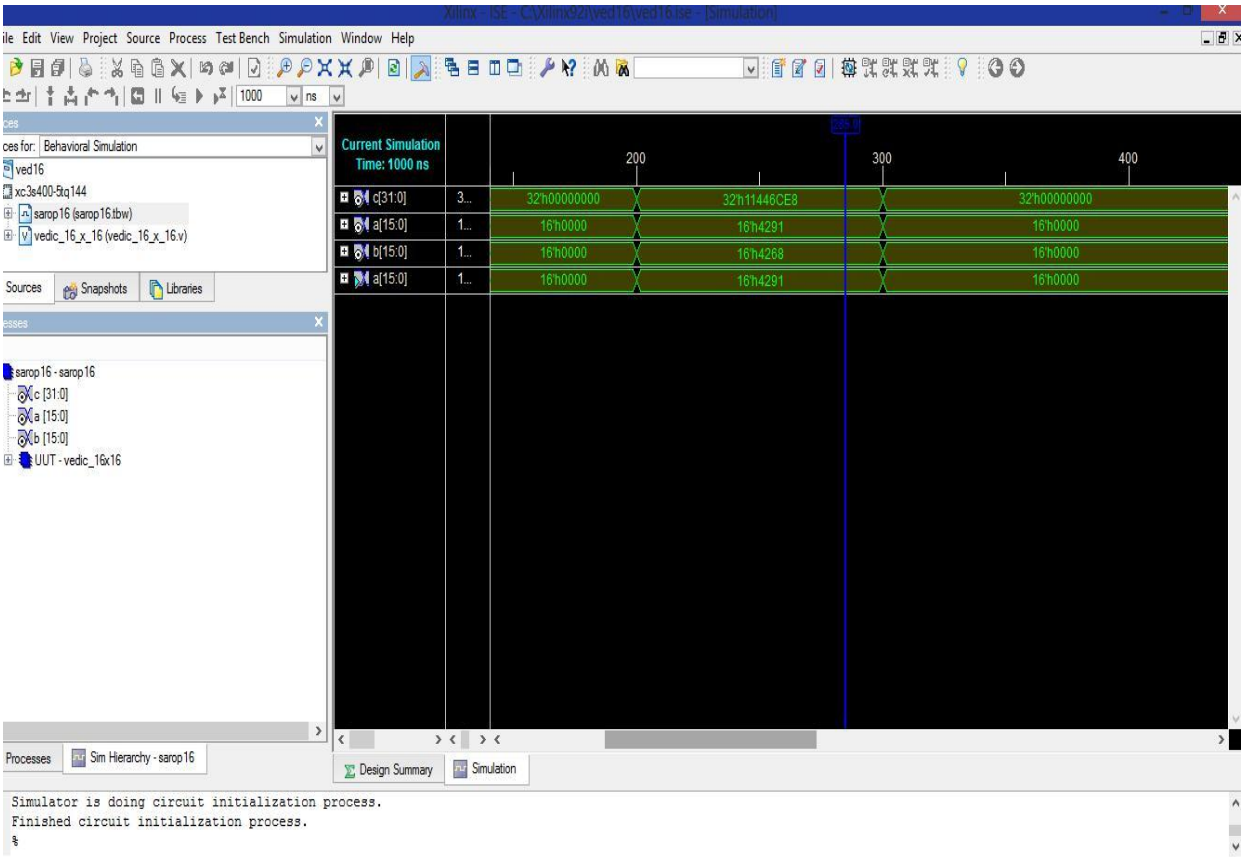

Fig3.Simulation output of Vedic multiplier

The above Simulation Result illustrates the inputs 4291H and 4268H for a and b inputs respectively fed to a 16x16 bit Vedic Multiplier to obtain output at the c variable as 32'h 11446CE8.7.4 Power Estimation

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 8, Issue 6, June 2019

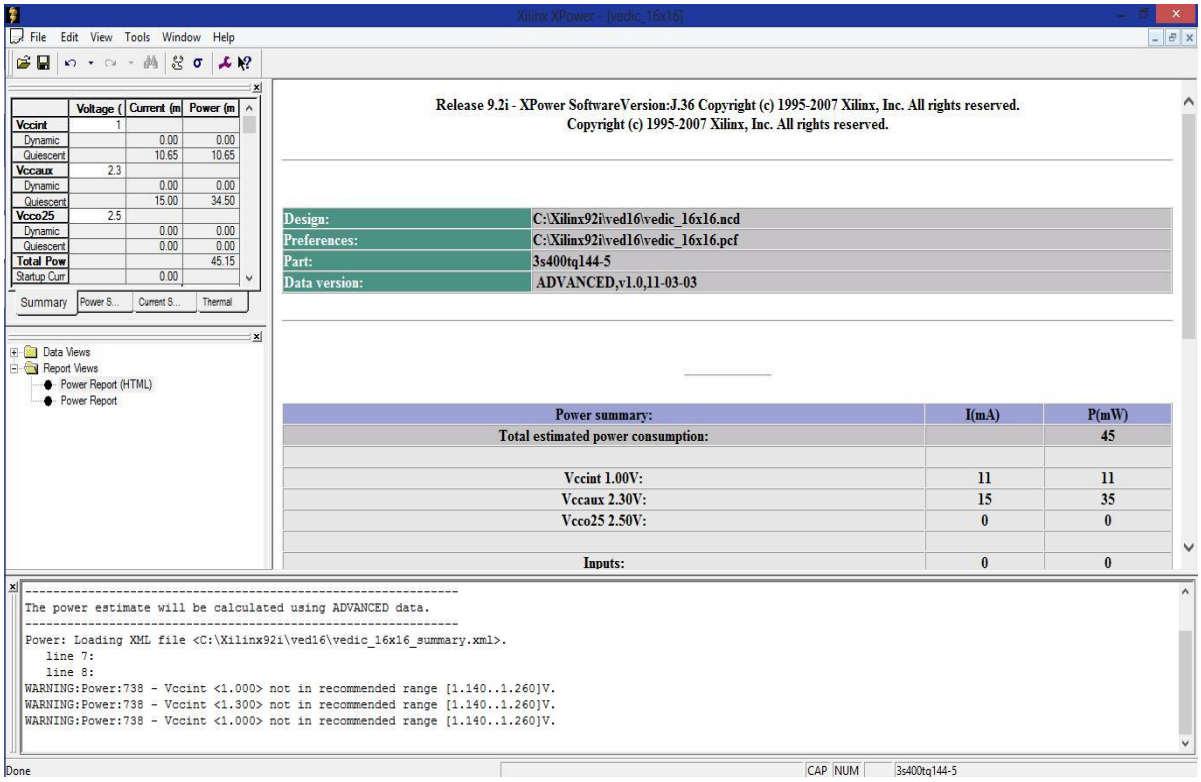

Fig4.XPower Analyzer Power Output of 16x16 Vedic Multiplier

III. TIMING SUMMARY

Speed grade: -5

Maximum combinational path delay: 32.515ns

Device utilization summary

Selected Device :	3s400tq144-5			
Number of Slices:	355	out of	3584	9%
Number of 4 input LUTs:	626	out of	7168	8%
Number of IOs:	64			
Number of bonded IOBs:	64 out of		97	65%

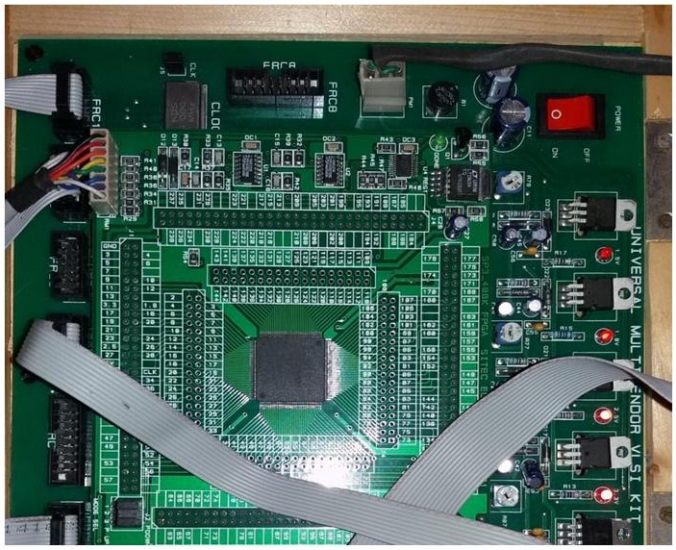

Fig.5.Hardware Implementation Output of 4 bit Vedic Multiplier

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 8, Issue 6, June 2019

IV. CONCLUSION

This paper gives the new multiplier algorithm for the power reduction and minimum area utilization with reduction of time. This Vedic multiplier gives the result of 16x16 multiplication with reduced area and the power consumption is 45mw.The future scope is to implement the 32x32 bit multiplication to reduce the area and power with reduced clock frequency.

REFERENCES

[1]. Vigneshwaran, K., Muruganantham.T,2015,Low-complexity matrix inversion algorithm for high throughput data detection in the hyper MIMO reverse channel in International Journal of Applied Engineering Research

[2]. Abhijith Kini G. September 2011. "Asynchronous Hybrid Kogge-Stone Structure Carry Select Adder Based IEEE-754 Double-Precision Floating-Point Adder" Department of Electronics & Communication Engineering, National Institute of Technology Karnataka, NITK-Surathkal. Surathkal, Karnataka 575025, India.

[3]. Shamim Akhter, "VHDL Implementation of Fast NXN Multiplier Based on Vedic Mathematics", Jaypee Institute of Information Technology University, Noida, 201307 UP, INDIA, 2007 IEEE.

[4]. Abhijeet Kumar, Dilip Kumar, Siddhi, "Hardware Implementation of 16*16 bit Multiplier and Square using Vedic Mathematics", Design Engineer, CDAC, Mohali.