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# Comparative Analysis and Behavior of Digital Applications simulated using MOSFET, CNTFET and FinFET Transistors in HSPICE

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**Abstract:** Full Adder constitutes elementary building block for advanced digital applications. SRAM is a runtime memory unit which performs fast read and write operations. These digital applications dissipate considerable power when synthesized using MOS. FinFET and CNTFET implementations of these circuits have improved power dissipation, delay & scalability characteristics over MOSFET, The HSPICE tool by Synopses designs logical and arithmetic applications and analyse power delay behavior. Library files for coding of FinFET are provided by BSIM & for CNTFET are provided by Stanford Library. Input /Output waveforms have been provided for both applications.

**Keywords:** FinFET, Nano tubes, CNTFET, SRAM, Full Adders

## I. INTRODUCTION

As the miniaturization reached nanometer level with the increasing need of compact faster processing circuits, shrunken MOSFETs suffer from reliability problems because of excessive heating. The thin body MOSFET is the backbone of FinFET. Scaled MOSFET channel length when reduced below a critical value decreased the gate control over the channel. Also increases the power dissipation. As per the structure, FinFET is a double gate MOSFET, to control the channel and offers distinct advantages for scaling into very short gate lengths. The two gates together strongly influence the channel potential, combating the drain impact, and leading to the better ability to shut off the channel current, reducing Drain Induced Barrier Lowering (DIBL). The Short Channel Effect (SCE) can be suppressed and the power dissipation can be reduced by decreasing the fin width (Tfin). This is reported by P.C.Rajashree et al[1].
'CNTFET' uses 'CNT' as their semiconducting channels. A 'Single-Wall CNT' (SWCNT) made up of one cylinder only. This makes fabrication of these device easier Assessment of performance begins with the analysis in basic or simple circuit blockshence they are first implemented in Full Adder which forms the basis of arithematic electronics. Full adder implementation is followed by SRAM cell analysis when implemented with MOS and FinFET.

## II. SIMULATION TOOL

'SPICE' stands for "Simulation Program with Integrated Circuits Emphasis". It's a powerful tool with innumerous libraries to simulate electrical circuits. From the steady-state, transient, to frequency domains all the analysis can be done easily. Its Netlist file contains the node configuration. The file has '.SP extension'. Secondly the model files are there in Netlist. The transistor, diode etc electronic component implementation using MOS, FinFET are there in model files of the simulator as mentioned in K.Skundert et al[3].The netlist code is then browsed and added to "HSPUI" (HSPICE User Interface) .Finally the Waveforms are provided by the Avanwaves feature of HSPICE

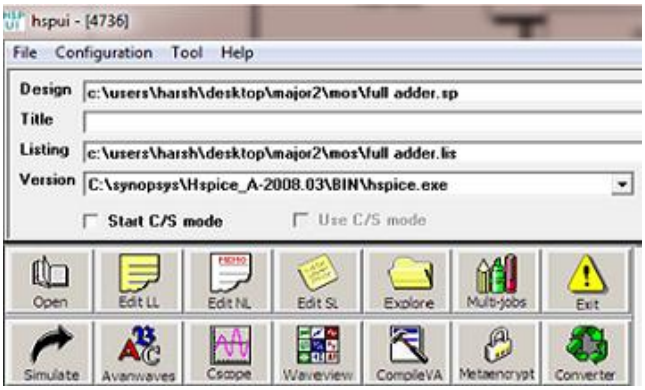

Fig (i) HSPICE user interface from Synopses(hspui)

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## III. DIGITAL APPLICATIONS

### A) Full Adder

The basic gates SOP and POS equation of full adder cannot be reduced using KMAP however full adder can be implemented using CMOS technology to reduce the gate count, delay in output etc. Few logical tricks are carried out to decrease the transistor count like utilizing partial output of sum for carry – generation circuits. However, this increases delay. Further studies led to the implementation of carry look ahead generator but then circuit complexity increased [2]. The figure(ii) shows the complementary static CMOS implementation of full adder, and the corresponding gate level implementation is shown in figure (iii). It requires 28 transistors. In addition to consuming a large area, this circuit is slow. We are using 28 transistor logics in our project.

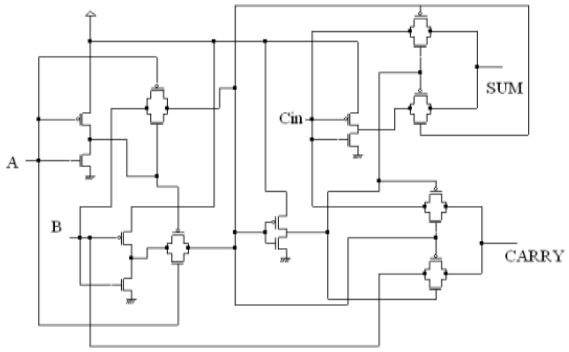


Fig. (ii) Full adder circuit implemented using Twenty Eight transistors in complementary configuration

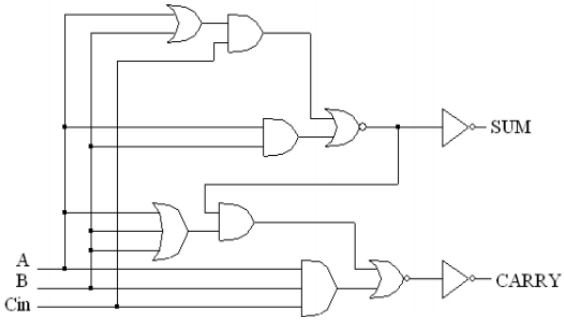


Fig (iii) Gate level implementation of Full adder designed using Twenty Eight CMOS Transistors

Table 1:Comparision of Performance (Full Adder)

| Transistor | Time Delay (sec) | Power Dissipation(W) |
|---|---|---|
| MOSFET | $9.368 \times 10^{-8}$ | $1.06 \times 10^{-6}$ |
| FinFET | $9.87 \times 10^{-9}$ | $1.909 \times 10^{-7}$ |
| CNTFET | $9.979 \times 10^{-9}$ | $3.059 \times 10^{-7}$ |

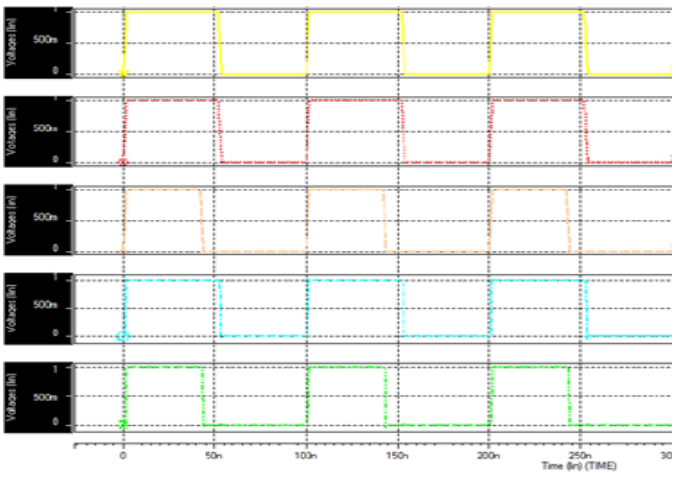

Fig.(iv) Input and output waveforms obtained using Avanwaves for the full adder design

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Table 2: I/O parameters for Fig.(iv)

| Symbol | Graph Color | Description |
|---|---|---|
| V(2) | Yellow | First Input |
| V(3) | Red | Second Input |
| V(4) | Brown | Carry Input |
| V(10) | Light Blue | Carry Output |
| V(18) | Green | Sum |

**b) 2 X 2 SRAM Memory**

SRAM has exhaustive implementation as temporary storage in computer which speeds its operations. The 2 X 2 SRAM Memory consists of two memory words, each having a size of two bits. Every bit is stored in a six transistor SRAM cell, working in two possible modes: Read and Write. Our prime focus in this project is to perform Write operation. The necessity condition for sustaining an SRAM cell is Strength(W/L) of Pull up Transistor(XM3,XM4) << Strength of Access Transistor(XM5,XM6) << Strength of Pull down Transistors(XM1,XM2). For the Write operation to write '0' Word line(W) should be high, bit line (b1/b2) =1, complementary bitline(c1/c2))=0. Later when word line(W) is low, the bit '0' stored in cell will be preserved at node Q[2]. This is depicted combinedly by fig (vi) and fig (iv). Here X1-X4 are the SRAM cells of fig (v).This is reported by Ravi Kumar et al[7]

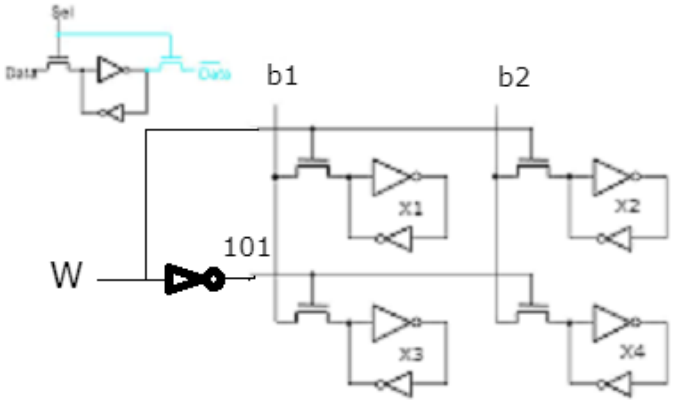


Fig.(v) 2 X 2 SRAM MEMORY UNIT

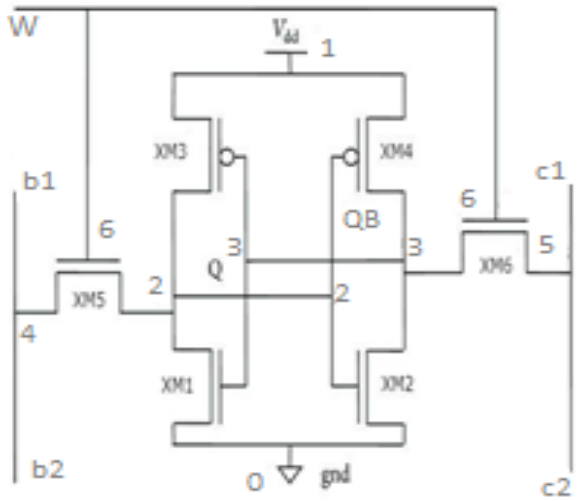


Fig.(vi) A bistable cross coupled SRAM using 6 Transistors

Table 3: Comparision of SRAM's Performance

| Transistor | Time Delay | Power Dissipation |
|---|---|---|
| MOSFET | $2.1888 \times 10^{-8}$ | $4.707 \times 10^{-5}$ |
| FinFET | $4.4163 \times 10^{-9}$ | $4.7376 \times 10^{-6}$ |

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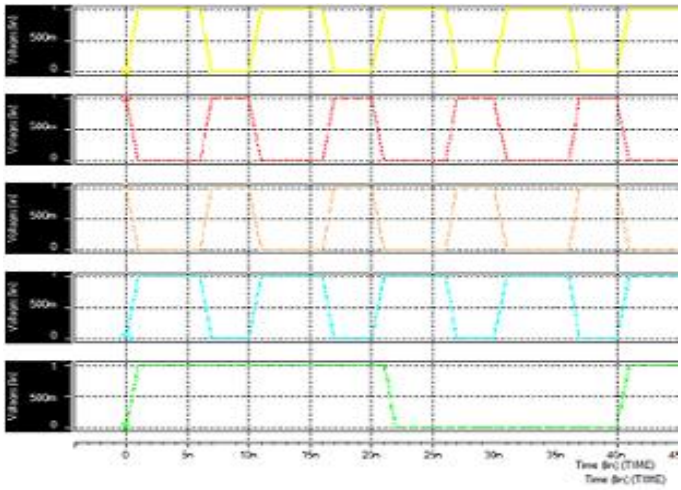

Fig. (vii) Input waveform obtained using Avanwaves for 2X2 SRAM Memory unit

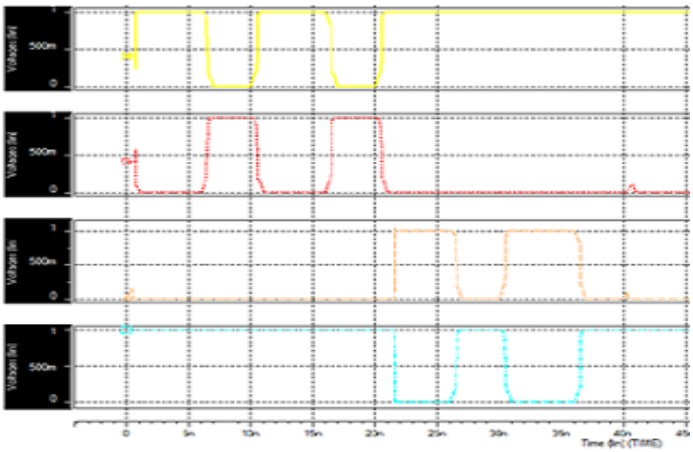

Fig. (viii) Output Waveformfrom Avanwavefor 2X2 SRAM Memory unit

Table 4: Relevent data for fig (vii)

| Symb. | Graph Color | Description |
|---|---|---|
| V(b1) | Yellow | Read Input to the First bit [BL] |
| V(c1) | Red | Complementry Read Input to the First bit [BLB] |
| V(b2) | Orange | Read Input to the Second bit [BL] |
| V(c2) | Blue | Complementry Read Input to the Second bit |
| V(w) | Green | Write Input to the First word(X1,X2 ) [WL] |

Table5: Important information for fig. (viii)

| Symbol | Graph Color | Description |
|---|---|---|
| V(q1) | Yellow | Data written in X1 |
| V(q0) | Red | Data written in X2 |
| V(p1) | Brown | Data written in X3 |
| V(p0) | Blue | Data written in X4 |

## IV. CONCLUSION

The results read aloud that FinFET and CNFET Full adder circuits have faster response than their MOSFET counterpart. However FinFET and CNTFET circuits have nearly same response speed. Also Power dissipation of FinFET adder is five times lesser than MOSFET implementation and is little below CNTFET implementation. Power dissipation in MOSFET based SRAM array is almost Ten times its FinFET counterpart. FinFET response is faster with delay in picoseconds. The delay in the MOS based SRAM is almost Ten times.

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