IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Vol. 10, Issue 6, June 2021

DOI 10.17148/IJARCCE.2021.10661

Power Optimization in Multiplier using VHDL

Mr.N. S. Panchbudhe, Mr.Rishab Golecha,Dr.Pradnya R. Morey

Assistant Prof. in DBACER,Nagpur

Wes Consultancy , Raipur

Assistant Prof. in DBACER,Nagpur

Abstract- In the recent year growth of the portable electronics is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like, DSP processor, math processor and in various scientific applications. Overall performance of these devices is strongly depends on the arithmetic circuits like multiplier. This paper presented detailed analysis of low power CMOS multiplier which is very important for today's scientific application. Experimental results show that it saves 10% of power for random input. Higher power reduction can be achieved if the operands contain more 0's than 1's.

I. INTRODUCTION

Multiplication is an essential arithmetic operation for common DSP applications, such as filtering and fast Fourier transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP systems.

CMOS is currently the dominant technology in digital VLSI. Two components contribute to the power dissipation in CMOS circuits. The static dissipation is due to leakage current, while dynamic power dissipation is due to switching transient current as well as charging and discharging of load capacitances. Since the amount of leakage current is usually small, the major source of power dissipation in CMOS circuits is the dynamic power dissipation. Dynamic power dissipation appears only when a CMOS gate switches from one stable state to another. Thus, the power consumption can be reduced if one can reduce the switching activity of a given logic circuit without changing its function.

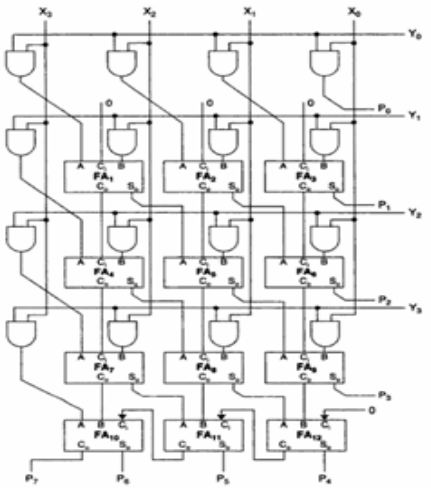

fig.1 Braun Muliplier

The bypassing scheme disables the operation in some rows or columns to reduce the power dissipation. For the parallel multiplier, the array implementation is the Braun's design. The components used in the Braun's design are full adder as well as AND gates.

Consider the multiplication of two unsigned n-bit numbers, where X = xn-1, xn-2, … x0 is the multiplicand and Y = yn-1,yn-2,……,y0 is the multiplier. The product of these two bits can be written as ;

$$P = \sum_{i=0}^{n-1} Xi \sum_{i=0}^{n-1} Yj 2^{(i+j)}$$

Where;

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$\sum_{i=0}^{n-1} Xi2^i$ Multiplicand $\sum_{i=0}^{n-1} Yj2^j$ Multiplier

II. PROPOSED METHOD

(1) We propose a multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages to this approach. First, it eliminates the extra correcting circuit as shown in Fig. 2. Secondly, the modified FA is simpler than that used in the row-bypassing multiplier.(2) In the second multiplier design instead of using AND gate we are using OR gate .The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. NOR gates are used instead of AND in accordance with the De Morgan's Law:

A.B = (A' + B')' (1)

From (1), it is clear that if NOR gates are used, the inputs have to be complimented. While it takes 6 transistors to build AND/OR gate, only 4 transistors are used for NOR/NAND gate.

III. LOW POWER MULTIPLIER WITH COLUMN BYPASSING

For a low-power column-bypassing multiplier, the addition operations in the (i+1)th column can be bypassed if the bit, ai, in the multiplicand is 0, In the multiplier design shown in Fig(2), the modified FA is simpler than that in the row bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1multiplexer. As the bit, ai, in the multiplicand is 0, their inputs in the (i+1)th column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs.

The column bypassing multiplier (CBM) only needs two tri-state gates and one multiplexer in a adder cell. When yj is 0 then the corresponding diagonal cells are functioning unnecessarily. In all these cells the partial products xi × yj and the carry inputs are zero for i = 0,1,…, n-1 and this chain does not contribute to the formation of the product. Consequently, the sum output of the above cell can bypass this unimportant diagonal with the use of transmission gates. To achieve all of the above we can replace the Full Adder cell shown in —Figure 2(a) with the cell in —Figure 2(b) called the Full Adder Bypassing (FAB) cell. The transmission gates in the FAB cell lock the inputs of the full adder to prevent any transitions when y = 0, and a multiplexer propagates the sum input to the sum output. When y = 1, the sum output of the full adder is passed.

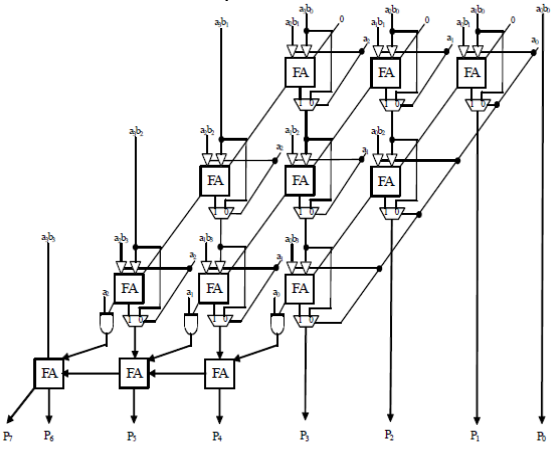

Fig 2: column bypassing

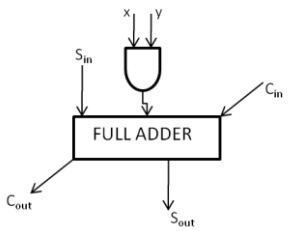

Fig2: (a)

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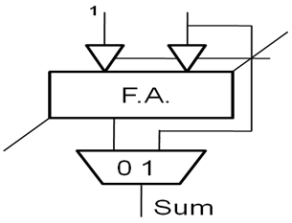


Fig2: (b)

A .Multiplier Design

The column bypassing multiplier is shown in Fig(1). Note that we only need two tri-state gates and one multiplexer in a modified adder cell. If aj=0, the FA will be disabled. We do not need a tri-state gate for the carry input (Ci-1, j), and the reason is given as follows. For a Braun multiplier, there are only two inputs for each FA in the first row (i.e. row 0). Therefore, when aj=0, the two inputs of FA0, j are disabled, and thus its output carry bit will not be changed. In the bottom of the CSA array, we need to set the carry outputs to be 0. Otherwise, the corresponding FAs may not produce the correct outputs since their inputs are disabled. This is done by adding an AND gate at the outputs of the last-row CSA adders. To understand the column bypassing technique, let's take an example of 4×4 multiplication as shown in Figure 2(c), which executes 1010*1111.

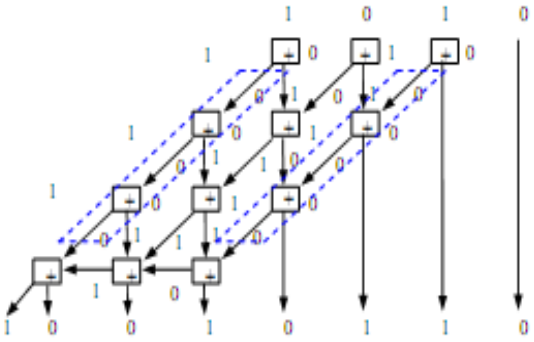


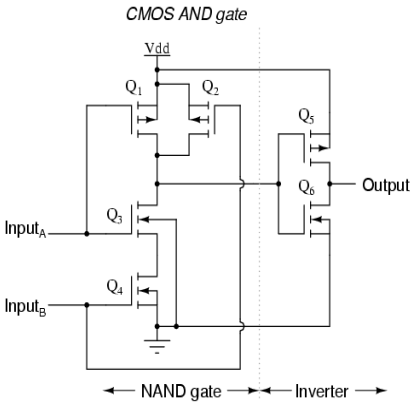
Fig 2(c): Multiplication in column bypassing

It can be verified that, for FAs in the first and third diagonals, two out of the three input bits are 0: the 'carry' bit from its upper right FA, and the partial product ai bj (note that a0=a2=0). As a result, the output carry bit of such an FA is 0, and the output sum bit is simply equal to the third bit, which is the 'sum' output of its upper FA.

IV. HARDWARE MODIFICATION

To design 4 x 4 multiplier we require 16 AND gates, of which each AND gate consists of 6 transistor. The same hardware can neither replaced by NOR gate which consists of only 4 transistors .This reduction in hardware results into less power consumption.

Figure shows the circuit of CMOS AND gate and CMOS NOR gate.



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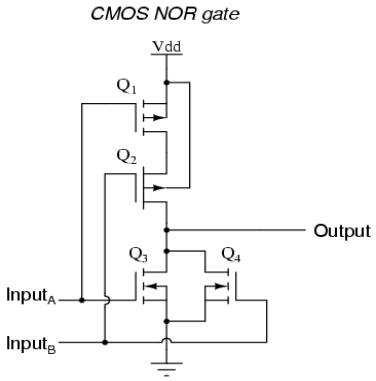

Thus, for a m* n multiplier, the proposed method introduces m + n extra inverters along with changing m*n AND gates to m*n NOR gates, effectively saving (m*n − (m + n)) inverters or 2*(m* n − (m+n)) transistors. Figure(3) shows proposed multiplier design with the replacement of AND gate with a NOR gate in a brown multiplier, resulting into requirement of less no. of transistor than the conventional design. This reduction in the hardware results into less power consumption and ultimately helps in a power optimization.

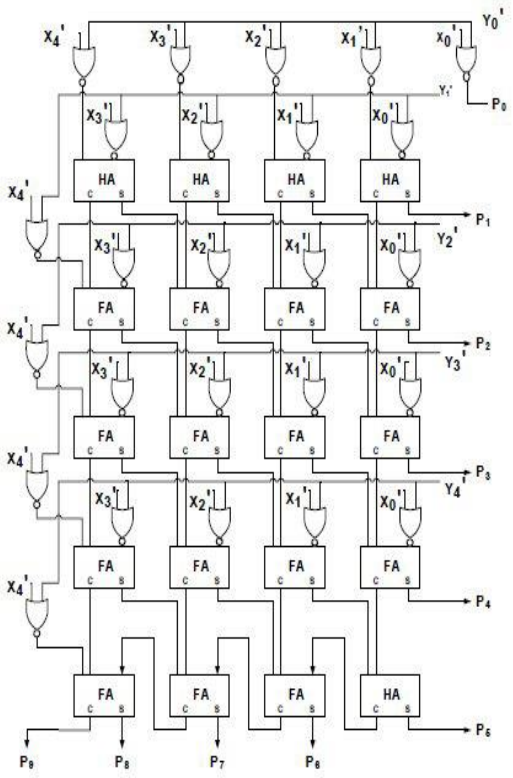

Figure 3. Proposed unsigned array multiplier

V. RESULTS

To evaluate the performance of this low-power multiplier, we implement the design with VHDL. We compare the performance of this design with a normal Braun multiplier the results are given as follows. Table 1 gives the expected power consumption by the three designs. In this experiment, the input patterns are assumed to be random, i.e. the probability of 0 and 1 are both 0.5. Note that this is a relatively pessimistic estimation. If the operands are sparse (i.e. the number of 0's is more than 1's), there will be greater power saving. Our results show that the brown multipliers actually consume more power. Our design consumes less power in all cases, and the reduction increases as the size becomes larger. If the distribution of 0's and 1's is not uniform, we shall be able to achieve higher power saving.

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		Power consumption
Conventional	Brown multiplier	28 mW
Proposed Multiplier	Column bypassing technique	22 mW
	Hardware modification technique	18 mW

TABLE .I POWER COMPARISON BETWEEN CONVENTIONAL AND PROPOSED MULTIPLIER

VI. CONCLUSION

From the above table of comparison it is observed that in proposed multiplier the hardware modified multiplier consume less power comparatively other two , it means that this is best multiplier.

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