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A Review on Design and Implementation Of 6T SRAM Cell

Roshan Hegde[1], B Rahul[2], Gouri R G[3], Sujay[4], Sowjanya[5]

Student, Electronics & Communication Engineering, MITE, Moodabidri, India[1-4]

Assistant Professor, Electronics & Communication Engineering, MITE, Moodabidri, India[5]

Abstract: SRAM, or Static Random Access Memory, is one of the fundamental elements of the digital world. In general, it uses a tremendous quantity of energy. A lot of SRAM research is thus being done in the areas of power dispersion, RAM chip size, and supply voltage requirements. This work considers SRAM analysis for low power applications in terms of Static Distortion Margin, The Information Retention Voltage, which is Read Margin (RM), and Write Margin (WM). One of the most crucial factors in memory design is static noise margin (SNM), which has an impact on both read and write tolerance. The threshold voltages of the SRAM cell's negative oxide metal transistor (NMOS) and positive metal oxide semiconductor (PMOS) components are correlated with SNM. High Write and Read Snr Margin are also major design obstacles. The challenge of the 6T SRAM project using 180nm, 90nm and 45nm technologies at Cadence Virtuoso is to address the scaling challenges of SRAM designs and explore the possibilities offered by different technology nodes. The focus is on optimizing the performance and energy efficiency of the 6T SRAM cells considering the effects of scaling and process variation. The purpose of this project is to analyze the trade-offs between power consumption, access time, and stability at each technology node, identify optimal design configurations, and develop guidelines for efficient and reliable 6T SRAM design. By leveraging Cadence Virtuoso's capabilities, this project aims to provide valuable insight into the development of robust, high performance SRAM cells in 180nm, 90nm and 45nm technologies.

Keywords: Noise Margin, Read Margin, SRAM, 6T-SRAM, Virtuoso, Write Margin

I. INTRODUCTION

SRAM is a type of semiconductor memory that stores data using bistable circuits. Unlike dynamic memory technologies such as DRAM, SRAM does not require constant refreshing of data, making it faster and more power-efficient. SRAM is widely used in various electronic devices, particularly as cache memory in processors and controllers. SRAM cells are designed using CMOS technology, which offers several advantages such as low power consumption, high noise immunity, and compatibility with integrated circuit fabrication processes. The basic building block of SRAM is a flip-flop circuit, typically implemented using six transistors (hence the term 6T SRAM cell). This configuration provides stability to store a bit of data without the need for constant refreshing. Although SRAM has a higher cost and lower density compared to DRAM, it offers superior performance and reliability. SRAM is commonly found in a range of electronic devices, including computers, smartphones, networking equipment, and automotive systems. As technology continues to advance, SRAM plays a critical role in meeting the demands for faster and more efficient data storage and access in various industries.

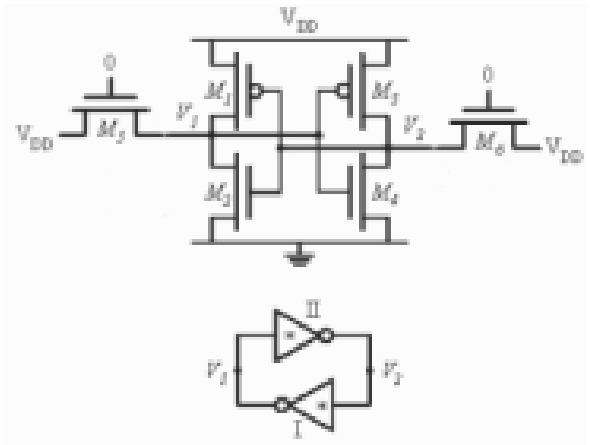

Fig 1.1 SRAM Transistor and FlipFlop

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II. LITERATURE REVIEW

Soumya Gadag et al.,[1] The research on the critical issue of power consumption reduction in VLSI (Very Large-Scale Integration). To reduce power loss, they used strategies like sleep and stacking. The design was developed using 0.18um CMOS based technology, and the power dissipation was assessed using the micro wind tool at the BSIM4 level. Surprisingly, their technique yielded a notable 40% reduction in overall power dissipation when compared to the typical 6T SRAM cell. This reduction in power usage is an important development in VLSI design since it leads to greater energy efficiency and battery life in electronic products. The study's findings emphasize the usefulness of their method in minimizing power-related difficulties and improving overall performance.

Michael C. Wang et al.,[2] Proposed a paradoxical method for lowering power consumption for SRAM operations. They advocated employing two distinct word lines (WL) as well as one WL linked to the cell's transistor. This technology aims to reduce switching power on the word line (WL) and bit line (BL), resulting in lower overall power consumption. The success of this strategy was proven by simulated outputs, which showed a considerable reduction in power consumption when using two WLs in SRAM operations. Their technique, which optimizes the switching strategy and reduces power dissipation, has the potential to improve energy efficiency in SRAM designs and the overall performance of memory systems. Their study's findings help to continue attempts to reduce electricity uses.

Michel Stuchi et al.,[3] They evaluated the read stability of the N curve metrics with the Static Noise Margin (SNM) in their study. The write ability was also compared using N curve measurements and standard approaches. Analytical methods were created to evaluate these indicators. According to the findings, VDD scaling did not interfere with read stability. The output of the N curve metrics was compared to both worst-case and corner-case designs. The study sought to assess the efficacy of N curve metrics in terms of read stability and write ability. The findings emphasized the benefits of employing N curve parametersto evaluate read stability and write capabilities in SRAM architectures. Using analytical techniques.

Akshay Bhaskar et al.,[4] Research was to reduce power consumption and delay in SRAM write operations. They used two approaches to do this: Gated VDD and MTCMOS. Their research found that the MTCMOS technology reduced power usage by 38.1% when compared to standard 6T SRAM. It also improved speed by 18.18%. In comparison to the typical 6T SRAM, the Gated VDD design consumed 16.18% less power and performed 13.03% faster. These findings illustrate the effectiveness of both strategies in decreasing power consumption and enhancing performance in SRAM write operations. The deployment of Gated VDD and MTCMOS gives valuable strategies.

Mukesh Kumar et al.,[5] Reviewed and compared 6T, 7T, and 8T SRAM cells using the gpdk180 technology. The study aimed to examine various parameters such as dynamic and static power, rise and fall time, delay, and bandwidth. The Cadencetool was used for the analysis. The study discovered that the static power consumption was the same for all three SRAM cell designs. However, the dynamic power consumption for the 7T SRAM was found to be 5.45uW and 10.26uW for the 8T SRAM, indicating that the 8T configuration consumes more power. The experiments were carried out at a temperature of 27°C.These findings shed light on the trade-offs between power consumption and performance for various SRAM cell designs.Researchers and designers can improve their results by evaluating these parameters.

Manoj Padmanabha Murthy. T et al.,[6] Researchers compare the design and performance of SRAM cells in 180nm and 45nm technologies. SRAM is a high-speed semiconductor memory that uses bistable circuits to store 1 bit of data and does not require refresh circuits like DRAM. Because of its fast data access, it is often employed as cache memory in processors and controllers. DRAM, as opposed to SRAM, is denser and is utilized in major memories where speed is less important. SRAM is finding new uses in industrial and automotive electronics. The thesis is concerned with reducing area by proposing compact layouts for peripherals such as pre-charge and sensing amplifiers. PVT analysis is used to assess the durability of the SRAM cell to modifications and to notice power fluctuations. Furthermore, the power values are compared when the width of the channel is doubled or tripled.

Changhwan Shin et al.,[7] The efficiency and threshold voltage variability of completely depleted silicon-on-insulator (FD SOI) MOSFETs are compared to conventional bulk MOSFETs in this study. The authors examine the characteristics of these two types of MOSFETs using 3-D device modeling with atomistic doping profiles. The operating measurements of a six transistor SRAM cell at the 22 nm CMOS semiconductor node are then estimated using compact modeling. The research looks at how cell ratio, pull-up ratio, and operating voltage affect read and write margins as well as read current in FD-SOI and bulk SRAM cells. The yield and cell-area advantages of FD-SOI technology are investigated using iso-area and iso-yield comparisons. Furthermore, the study compares the minimum operating voltages (Vmin) required for FD-SOI and bulk SRAM cells to meet

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Rajasekhar Keerthi et al.,[8] In this research, a seven-transistor (7T) SRAM cell is used and compared to a typical six-transistor (6T) SRAM cell to address read data destruction and improve stability at LOW-VDD. The solid functioning of an 8-bit SRAM, also known, is demonstrated using statistical models and data analysis, considering variations in the process and mismatch. The measurement results indicate that the stationary noise margin (SNM) of the 7T SRAM cell matches that of the 6T SRAM cell. In addition, the stability of the 8-bit 7T SRAM at IOW-VDD has been demonstrated by properly testing the SRAM at 720 mV, which highlights its improved reliability and performance over the 6T SRAM.

Christensen D.C. et al.,[9] They studied the Static Noise Margin (SNM) of a 6T Static Random Access Memory (SRAM) cell developed in 90-nm CMOS technology. The research entails modeling the SRAM cell and analyzing the noise margins while adjusting various parameters that influence SRAM operations. Temperature, threshold voltage, power supply voltage, cell ratio, pull-up ratio, and the process corner changes are among the parameters. The results of the simulation are compared to the square law device concept given by Seevinck. The study's findings show that the computer simulation results match the model, proving the model's validity in predicting the behavior of the SRAM cell under various operating situations. This study adds to our understanding of and optimization of 6T SNM.

Pandurang Vemula et al.,[10] Reviewed in detail about increased use of SRAM and CMOS technology in processors and system-on-a-chip (SoC) devices, new design innovations are necessary for SRAM to keep up with scaling. SRAM bit cells, which are made up of the smallest geometric devices, seek for high density but are sensitive to technical scaling. The successful implementation of SRAM is critical to the success of future technologies. Several SRAM bit cell topologies and array layouts have been proposed to address concerns such as poor stability, process variation tolerance, device aging, and soft errors. This chapter addresses the function of SRAM in current computer systems, peripheral circuitries, and various SRAM bit cell topologies, as well as their benefits and drawbacks.

Benton H. Calhoun et al.,[11] Discussing the importance of saving power in memory design develops, there is a trend to functioning synapses at less available voltages. Investigations into sub-threshold operations for logic have revealed the possibility of low-energy operation in this region. This proposes a point of convergence for energy-constrained programmers, where SRAM can run at subthreshold voltages compatible with logic. Sub-threshold voltages, on the other hand, limit the static noise margin (SNM), making it critical to understand the impact of design decisions and other parameters. This article investigates SNM for sub-threshold bit cells in a 65-nm manipulator, looking at the impacts of size, DD, temperature, and threshold change. The findings show the large impact of variance on SNM and provide a methodology for estimating SNM throughout the most adverse distribution tail.

Gourav Arora et al.,[12] The analysis of establishing a high Read and Write Noise Margin in SRAM design is the topic of this study. It compares the read and write stability and ability of 6T and 7T SRAM cell architectures across technologies. The investigation focuses on the Static Noise Margin (SNM), which affects both the read and write margins. The article compares the Read Noise Margin (RNM) and Write Noise Margin (WNM) of both SRAM cell types in the paper. Using the Tanner EDA tool, the results reveal that the 7T SRAM cell outperforms the 6T SRAM cell by providing larger read and write noise margins across several CMOS technologies (45nm, 32nm, and 22nm).

Arshad Moradi et al.,[13] Evaluated a novel technique for increasing the margin of the 6T-SRAM cell in their study. The proposed method decreases the amount of space occupied by the subthreshold SRAM cell while enhancing its write cycle. This is accomplished by employing a PMOS-stacked network, which avoids the need for a write cycle.

Shweta Gupta et al.,[14] Have focused on minimizing leakage current in SRAM cells spanning various semiconductor technologies. The researchers investigate three source-biasing strategies to reduce power loss in the 6T SRAM device. These techniques involve the NMOS semiconductor clamping, PMOS diode securing and NMOS-PMOS diode clamp at 45 nm and 90 nm technology. Furthermore, the article highlights the fabrication of a 6T SRAM cell using the multiple threshold CMOS (MTCMOS) method at the 45 nm technology node. The simulations are run using supply voltages of 0.95 V and 0.45 V corresponding to the 90 nm and 45 nm technology, accordingly. The researchers hope to effectively reduce leakage current by investigating these strategies and technologies.

Teijo Lehtonen et al.,[15] The detailed investigation of the study on using the Near-Threshold Computing (NTC) method to minimize power consumption in CMOS devices, specifically in the design of low-power cache memory circuits. Caches are known to consume a big amount of power and take up a significant amount of space in these kinds of systems, making their use of energy an important element in total system power efficiency. To solve this, the researchers examine the efficacy of 6T and 8T cells of SRAM to determine which is best for cache memory circuits. According to the data, the 8T SRAM cell is more reliable than the 6T SRAM cell. The paper intends to achieve considerable reductions by using NTC and selecting more trustworthy 8T SRAM cells.

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G. Shivaprakash et al.,[16] Examine the emphasizes the analysis of SRAM for applications that require little power, taking into account SRAM's critical position as a key component in the digital world. The paper specifically computes the Dramatic Read Voltage (DRV) for a 6T-SRAM cell optimized for high-speed applications. A 6T-SRAM design constructed in 90nm technology is subjected to performance study. SRAM is known for using a huge quantity of power and taking up an important portion of diarrhea. The Static Interference Margin (SNM) has been recognized as a significant characteristic in SRAM cells that affects both read and write margins. The threshold values of the NMOS and PMOS transistors within the SRAM cell are directly related to SNM. The researchers hope to learn more about these qualities by analyzing their paper.

Kavita Khare et al.,[17] Demonstrated the realization of a 6T SRAM cell that has shorter reading and writing times, region, and energy use. The researchers show that using greater cell ratios may improve read and write time while boosting stability. The approach involves employing global bit lines to reduce energy use while increasing memory capacity. The study explicitly builds two SRAM cells for a 4 Kb storage core working at 1.8V supply voltage. However, it should be observed that increasing the capacity of memory also increases bit-line parasitic capacitance. This can lead to slower power sensing and higher energy consumption. By tackling these issues, scientists hope to improve the productivity and effectiveness of SRAM cells.

Budhaditya Majumdar et al.,[18] Present a unique CMOS 6-transistor SRAM cell built primarily for independent and low power application in embedded systems. The suggested cell does not require a refresh cycle because it stores data via current leaked and positive feedback. Surprisingly, the new cell is the same size as a normal six-transistor cell using identical techniques and design requirements. However, as compared to conventional architectures, it considerably improves energy consumption and read stability. This revolutionary CMOS 6-transistor SRAM cell offers a viable option for improving performance while remaining compact, making it suited for a wide range of low-power and mobile devices.

Nahid Rahman et al.,[19] The issues experienced by static memory (SRAM) circuits owing to size decreased in System-On Chip (SoC) along with other integrated devices are explored in the study performed by Nahid Rahman, B. P. Singh et al. The requirement for better density in devices running at lower supply energies is driving the decrease of SRAM size. While this scaling allows for power savings, it has an influence on the performance and stability of SRAM circuits. The study, which focuses on the 45nm manufacturing node, gives vital insights to the stability difficulties and noise impacts experienced by traditional 6T SRAM cells as a result of supply voltage scaling. The study improves awareness of SRAM cell behavior and suggests potential techniques for improving safety during low-voltage operation.

Hiroyuki Yamauch et al.,[20] This study examines the effects of various fin patterns on the electrical properties of hybrid Tunnel Field-Effect Transistors (TFETs) and assesses how well they function in comparison to hybrid TFETs with other fin shapes. The goal is to create fast, low-power devices for nanoelectronics technologies in the future. In comparison to traditional MOSFETs, TFET technology delivers greater leakage current reduction due to its tunnel switching capacity. The study examines the gate range of coverage of different fin designs with the goal of reducing leakage currents. Electrical properties for various fin shapes of TFETs, including drive current, leakage current, and subthreshold slope, are calculated using the TCAD simulation programmed. This shows TFETS functions better

III. SUMMARY

Depending on the manufacturing node employed, such as 180nm, 90nm, or 45nm, the electrical load of a 6T SRAM cell architecture varies. In this examination, we will use Cadence Virtuoso to examine the electricity consumption metrics of 6T SRAM cells for every one of these nodes. The power cost of the 6T SRAM cell architecture at the 180 nm technology node is somewhat greater than at more recent nodes. Greater transistor sizes and greater currents of leakage are to blame for this. Static usage of electricity, which includes sub threshold leaky and gate loss currents, accounts for most of the power dissipation. When compared to nodes of subsequent technologies, the dynamic power use that happens during both writing and reading actions is substantially lower. Cadence Virtuoso offers several capabilities for power analysis that SRAM cell architecture varies. In this examination, we will use Cadence Virtuoso to examine the electricity consumption metrics of 6T SRAM cells for every one of these nodes. The power cost of the 6T SRAM cell architecture at the 180 nm technology node is somewhat greater than at more recent nodes. Greater transistor sizes and greater currents of leakage are to blame for this. Static usage of electricity, which includes sub threshold leaky and gate loss currents, accounts for most of the power dissipation. When compared to nodes of subsequent technologies, the dynamic power use that happens during both writing and reading actions is substantially lower. Cadence Virtuoso offers several capabilities for power analysis that are considered as best among them.

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IV. CONCLUSION

The exact objectives, goals, and performance criteria of the design would determine the outcomes for a 6T SRAM cell developed using Cadence Virtuoso software in multiple technologies employing 180nm, 45nm, and 90nm. However, the following broad conclusions can be based on. Stability is a 6T SRAM cell intended to keep data storage steady. By utilizing the feedback loop, its cross-coupled inverter pair assures the storage of an illogical value. The process of implementing using Cadence Virtuoso validates the cell's stability, reducing the possibility of data loss or modification. Operations for Read and Write: The 6T SRAM cell enables quick read and write procedures. The access transistors make it possible to read the data from storage without significantly altering the state of the cell. The write transistors also make it possible to change the data that has been saved without interfering with other cells in the array. Noise Margin: Cadence Virtuoso's implementation enables examination of the noise margin, a metric for the SRAM cell's resistance to noise. An improved capacity to withstand outside forces without making mistakes is indicated by a greater noise margin. The design may be made more reliable by optimizing it to provide a reasonable noise buffer.

Reduced Leakage Current: The 45nm technological scale benefits from improved process optimizations, including cutting-edge gate topologies and materials. Lower power consumption results from these improvements' successful reduction of transistor leakage currents. The 45nm node displays much lower leakage currents as compared to larger technological nodes like 180nm and 90nm, which boosts power efficiency.

Smaller Feature Size: The transistor size of the 45nm technology node is smaller than that of the 180nm and 90nm nodes. The energy needed to charge along with discharge the nodes that are used during reading and writing operations reduces as the transistor's capacitance grows smaller. The power consumption of 6T SRAM cells is reduced as a result of these smaller feature sizes.

Total Power reductions: The 45nm technology node's improvements, which include decreased leakage currents, lower feature sizes, improved gate topologies, and increased transistor performance, all lead to sizable power reductions for 6T SRAM. The 45nm technology node exhibits the best power consumption characteristics when compared to the 180nm and 90nm nodes, making it the greatest option for applications where power efficiency is a crucial requirement. It is obvious from these metrics that the 45nm manufacturing node provides the optimum power usage effectiveness for 6T SRAM. When choosing a technological node, it is crucial to consider additional aspects like performance, space, and cost because these characteristics can change depending on the demands and limitations of a certain design.

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