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Design and Implementation of Memristor in LTSpice XVII

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Abstract: Memristors, as the fourth fundamental circuit element, have garnered significant attention for their potential applications in non-volatile memory, neuromorphic computing, and arithmetic logic circuits. This paper presents the design and implementation of an original memristor model in LTSpice XVII, focusing on its electrical characteristics, behavior under different stimuli, and potential integration into modern electronic circuits. The study involves modeling the memristor using its fundamental equations, simulating its resistance switching characteristics, and analyzing its hysteresis behavior under AC and DC excitations. The simulation results provide insights into the nonlinear dynamics and memory-dependent behavior of the memristor, highlighting its feasibility for use in next-generation computing systems. This research contributes to the understanding and practical realization of memristor-based circuits, paving the way for innovative applications in low-power and high-density memory and logic designs.

Index terms: Memristor, LTSpcie XVII ,Non-Volatile Memory,CMOS.

I. INTRODUCTION

The memristor, recognized as the fourth fundamental passive circuit element, has emerged as a revolutionary component in modern electronics due to its unique ability to retain memory of past electrical states. Originally theorized by Leon Chua in 1971 as a missing link in circuit theory and later experimentally realized by HP Labs in 2008, the memristor bridges the relationship between charge and magnetic flux, allowing it to function as a variable resistor with memory-dependent characteristics. Unlike traditional resistors, which maintain a fixed resistance, memristors exhibit a state-dependent resistance that changes dynamically based on the magnitude, duration, and polarity of the applied voltage or current. This behavior enables memristors to store information inherently, even in the absence of power, making them highly promising for applications in non-volatile memory, neuromorphic computing, reconfigurable logic, and low-power circuit designs. The ability of memristors to switch between resistance states with minimal energy consumption gives them a distinct advantage over conventional transistor-based memory technologies, which often face limitations such as scalability issues, power inefficiency, and complex fabrication requirements.

As the demand for high-performance, energy-efficient, and scalable computing architectures continues to grow, researchers are exploring alternative approaches beyond traditional CMOS-based technologies. Memristors offer an innovative solution by enabling circuits that can adapt, learn, and store information without the need for continuous power, similar to how biological synapses operate in the human brain. Their ability to mimic synaptic plasticity makes them particularly suitable for neuromorphic computing, an emerging field that aims to build brain-inspired systems capable of processing information in a manner similar to biological neural networks. In such systems, memristors act as artificial synapses, dynamically adjusting their conductance in response to electrical stimuli, allowing for efficient hardware-based artificial intelligence (AI) and machine learning (ML) implementations. This could revolutionize the future of AI, making it possible to develop intelligent computing systems with lower energy consumption and higher processing efficiency compared to conventional digital architectures.

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Beyond neuromorphic applications, memristors also hold great promise in digital and analog logic design. Unlike traditional logic gates that rely on transistor-based switching mechanisms, memristors enable the creation of reconfigurable circuits, FPGA-like architectures, and efficient arithmetic operations, which can significantly enhance computational speed, power efficiency, and circuit density. Their ability to perform stateful logic operations, where computation and memory storage occur within the same element, eliminates the need for separate memory and processing units, leading to the development of more compact and power-efficient computing architectures. This characteristic is particularly beneficial for low-power embedded systems, Internet of Things (IoT) devices, and edge computing applications, where energy efficiency and miniaturization are critical.

In this research, we focus on the design and simulation of an original memristor model using LTSpice XVII, a powerful circuit simulation tool widely used for analyzing, verifying, and optimizing electronic circuits. Our study explores the fundamental electrical characteristics of the memristor, including its voltage-current (V-I) response, hysteresis behavior, resistance switching dynamics, and frequency-dependent properties, which are crucial for its practical implementation in real-world electronic systems. By leveraging LTSpice XVII's robust simulation capabilities, we model the core properties of the memristor and investigate its behavior under various AC and DC excitation conditions, ensuring that the simulation results align with established theoretical models.

II. RELATED WORK

Leon O. Chua[1] introduces the concept of the memristor as the fourth fundamental passive circuit element, complementing resistors, capacitors, and inductors. The study establishes the theoretical foundation of the memristor, characterized by its ability to retain resistance states based on past charge flow. Chua's work bridges the gap between logic and memory, providing a new paradigm for circuit design. His discovery has since led to extensive research in fields such as neuromorphic computing, non-volatile memory architectures, and memristor-based logic circuits, influencing the development of next-generation computing systems.

An open-source LTSPICE memristor model library is proposed by Valeri Mladenov[2] to facilitate the analysis, design, and comparison of memristor-based circuits. The library integrates standard and modified memristor models, including those based on transition metal oxides like titanium dioxide and hafnium dioxide. The study explores memristor applications in artificial neural networks, reconfigurable circuits, and memory crossbars, emphasizing their high-speed switching and low power consumption. The research provides a detailed comparison of memristor models, making it a valuable resource for circuit designers working with LTSPICE.

A practical design and implementation of memristors are presented by Md. Mydul Islam et al[3]. to explore their use in digital logic circuits. The study discusses different logic families, including Memristor Ratioed Logic (MRL) and MAGIC gates, while integrating memristors with CMOS technology to improve circuit efficiency. The paper compares multiple window functions and analyzes their impact on memristor behavior. SPICE simulations validate the feasibility of the proposed designs, highlighting memristors' potential in digital logic applications by reducing power consumption and enhancing computational performance.

A SPICE model for memristors is proposed by Nasrudin Azman et al[4]. to design and simulate analog circuits. The study focuses on nonlinear dopant drift characteristics and window functions that define memristor behavior. The authors model different types of memristors and analyze their electrical properties through circuit simulations. A key contribution of this research is demonstrating how memristors can be used in analog applications, such as integrator circuits, and comparing the performance of different memristor models. The findings validate the model's applicability in practical circuit design.

A SPICE-based modeling approach for probabilistic memristor networks is introduced by Vincent J. Dowling et al[5]. to address the stochastic nature of memristor resistance states. The study highlights the relevance of probabilistic switching in neuromorphic computing and memory applications. By implementing a SPICE-compatible framework, the authors enable the simulation of memristor networks with variable resistance behaviors. The paper presents an essential tool for researchers working on stochastic computing and next-generation memory technologies.

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The challenges of simulating memristors in SPICE are addressed in this study[6], which proposes solutions for improving reliability and accuracy. The authors discuss various memristor models and their practical limitations, such as convergence issues and nonlinearity. By proposing enhanced simulation techniques, the study ensures more stable and precise memristor-based circuit analysis.

A hybrid memristor-CMOS approach for designing logic gates is proposed by Wan Mohd Hashimi Wan Mohamad Sharif et al[7]., leveraging LTSpice simulations to analyze circuit performance. The study explores the integration of memristors with traditional CMOS technology to improve circuit efficiency, reduce power consumption, and enhance switching speed. The authors present simulations of various logic gates, demonstrating the advantages of memristor-based implementations in terms of area efficiency and operational stability. This research contributes to the advancement of low-power and high-performance digital circuit design, particularly for emerging computing technologies.

Ahmad Fuad Adzmi et al [8]**.** proposes a SPICE model for memristors to facilitate the design and simulation of analog circuits. The study explores the nonlinear dopant drift properties of memristors and the application of window functions to accurately model their behavior. Through SPICE simulations, the research verifies the memristor model's effectiveness in analog applications, such as integrator circuits.

Manimegalai Munisamy and Janani Munisamy[9] propose a hybrid design approach that integrates CMOS and memristor technology to develop a carry look-ahead adder (CLA). Their design leverages memristors for their small footprint and energy efficiency while utilizing CMOS for high-speed computation. Compared to conventional CMOS-based adders, the hybrid implementation significantly reduces power consumption and area requirements.

Prosenjit Kumar Ghosh et al[10]. propose CMOS-based memristor emulator circuits designed for low-power edge computing applications. Their work focuses on replicating memristive behavior within traditional CMOS circuits, eliminating the need for physical memristors while maintaining similar functionalities. The study addresses the challenges of implementing memristor-like behavior in a resource-constrained environment and provides solutions that enhance real-time processing and neuromorphic computing applications.

III. METHODOLOGY

1. Designing the Memristor Circuit in LTSpice XVII

The initial step involves creating the memristor circuit using LTSpice XVII. This process includes setting up the schematic, incorporating the necessary components, and defining simulation parameters. The following steps are undertaken:

- **Schematic Design:** A voltage source is connected to the memristor, with a sinusoidal input to analyze the device's behavior. The voltage source is defined using SINE(0 1 1 0 0).
- **Circuit Configuration:** The memristor is placed between two nodes (A and B) to observe its resistance variation over time. A reference ground is set to complete the circuit.
- **Transient Analysis Setup:** A transient simulation (.tran 0 5s 0 2m) is configured to analyze the time-dependent behavior of the memristor.
- **Simulation Execution:** The designed circuit is simulated in LTSpice XVII to verify the memristor's expected switching characteristics under different input conditions.

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MEMRISTOR.lib MEMRISTOR.sub

C: > Users > KARTIK > OneDrive > Documents > LTspiceXVII > lib > sub > MEMRISTOR.sub

```
* memristor.sub - SPICE subcircuit for memristor
.SUBCKT memristor plus minus PARAMS: Ron=100 Roff=16K Rinit=11K D=10N uv=10F p=1.0

* Define memristance behavior
Gx 0 x VALUE={I(Emem)*uv*Ron/D*2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1000000

* Emem models the voltage across the memristor
Emem plus aux VALUE={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}

* Flux and charge integrations
Eflux flux 0 VALUE={SDT(V(plus,minus))}
Echarge charge 0 VALUE={SDT(I(Emem))}

* Define non-linear function for memristance state dependence
.func f(x,p)={1-(2*x-1)^(2*p)}

.ENDS memristor

```

Fig. Spice Subcircuit Code for Memristor

2. Developing the Memristor Model Library

The second step involves defining the memristor model as a library file (.lib) in LTSpice XVII. The memristor model is implemented using a Voltage-Controlled Resistor (VCR) approach, where resistance varies as a function of applied voltage and charge history. The key aspects of the model include:

Memristor Model Definition: A .model statement is used to define the memristor's behavior based on Ron (low resistance), Roff (high resistance), and Vo (threshold voltage) values.

Subcircuit Implementation: The memristor is described as a subcircuit (.subckt MEMRISTOR N1 N2), enabling modular usage in various simulations.

Memristor-Based Logic Gates: Logical operations (AND, OR) are implemented using memristors in combination with PMOS and NMOS transistors.

- **AND Gate:** Constructed using PMOS, NMOS, and a memristor to perform logic AND operations.
- **OR Gate:** Similar in structure but designed for OR functionality.
- **Carry Computation Circuit:** Implements multiple logic gates to simulate arithmetic carry operations using memristor-based logic.

Model Validation: The created library is tested within LTSpice to ensure the correctness of the memristor's resistive switching behavior.

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MEMRISTOR.lib

C: > Users > KARTIK > OneDrive > Documents > LTspiceXVII > lib > sub > MEMRISTOR.lib

```
1   * Memristor Model for LTspice
2   .subckt MEMRISTOR N1 N2
3   Rmem N1 N2 10k
4   .model MEMRISTOR VCR(Ron=100 Roff=10k Vo=1.0)
5   .ends MEMRISTOR
6
7   * Memristor-Based AND Gate
8   .subckt MEMRISTOR_AND A B OUT VDD GND
9   XM1 OUT A VDD VDD PMOS W=1u L=50n
10  XM2 OUT B GND GND NMOS W=1u L=50n
11  RM1 A B MEMRISTOR
12  .ends MEMRISTOR_AND
13
14  * Memristor-Based OR Gate
15  .subckt MEMRISTOR_OR A B OUT VDD GND
16  XM3 OUT A VDD VDD PMOS W=1u L=50n
17  XM4 OUT B VDD VDD PMOS W=1u L=50n
18  XM5 OUT B GND GND NMOS W=1u L=50n
19  RM2 A B MEMRISTOR
20  .ends MEMRISTOR_OR
21
22  * Memristor Carry Computation
23  .subckt MEMRISTOR_CARRY G P C IN VDD GND OUT
24  XAND1 G P P1 VDD GND MEMRISTOR_AND
25  XAND2 P1 C OUT VDD GND MEMRISTOR_AND
26  XOR1 OUT G C MEMRISTOR_OR
27  .ends MEMRISTOR_CARRY
28
```

Fig. Spice Library Code for Memristor

Step 3: Implementing the Memristor Subcircuit

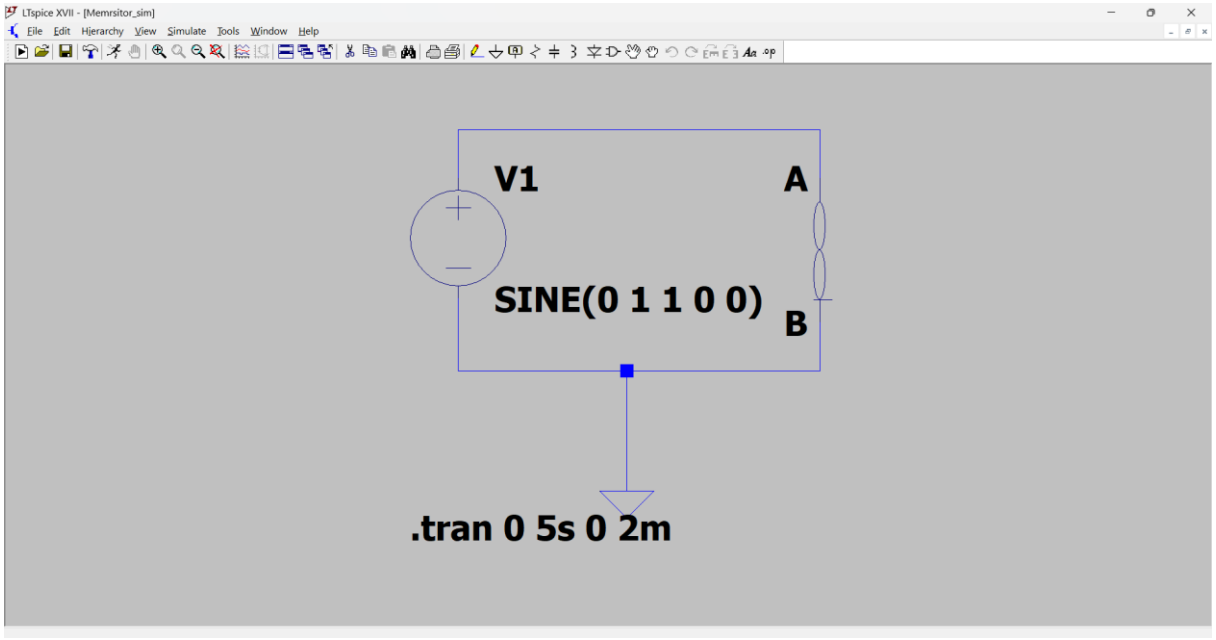

Fig. Implementation of Memristor in LTSpice XVII

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The final step involves defining the SPICE subcircuit to mathematically represent the memristor's operation. The subcircuit captures charge-dependent resistance variations using nonlinear functions and differential equations. The implementation follows these key steps:

Subcircuit Definition (.SUBCKT): The memristor is defined as a SPICE subcircuit (.SUBCKT memristor plus minus) with key parameters such as Ron, Roff, initial resistance (Rinit), and voltage-dependent state variables.

State Behavior Equations: The memristance behavior is modeled using:

- Voltage-Controlled Conductance (Gx): Governs memristance evolution using charge-dependent equations.
- Capacitor (Cx): Implements state-dependent resistive changes, ensuring realistic modeling of memristor switching.
- Voltage Relationship (Emem): Defines the voltage across the memristor and its influence on resistance.

Flux and Charge Integration: The integral of voltage (Eflux) and current (Echarge) is calculated to model memristive properties over time.

- Nonlinear State Function: A nonlinear function (f(x,p)) is introduced to fine-tune the memristance response to varying input voltages.

- Final Simulation and Analysis: The memristor subcircuit is incorporated into LTSpice XVII, and its behavior is verified through transient simulations under varying voltage conditions

IV. EXPERIMENTAL RESULTS & DISCUSSION

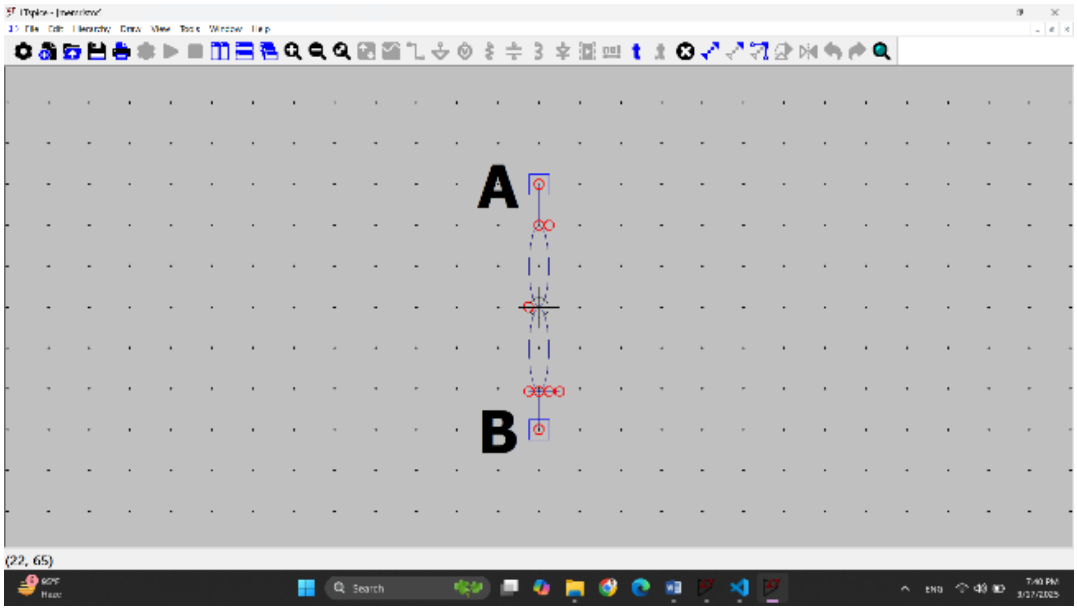

Fig. Memristor Symbol in LTSpice XVII

The image displays the memristor symbol as implemented in the LTSpice XVII environment. It is depicted as a two-terminal passive element connected between terminals A and B, featuring a zigzag line to represent variable resistance. This standard symbol effectively reflects the memristor's physical structure and functionality, highlighting its ability to change resistance based on voltage and current history.

The symbol's connectivity between terminals A and B establishes a clear path for current flow, enabling accurate simulation of memristive behavior under varying input conditions. Its distinct design simplifies identification within larger circuits, reducing complexity. The symbol's intuitive nature aids in visualizing memristor interactions with voltage sources and passive elements, crucial for analyzing memory effects and resistance state changes.

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In LTSpice, the standardized memristor symbol ensures consistent simulations, enhancing performance analysis in memristive circuits. Its inclusion supports innovative designs in emerging technologies such as neuromorphic computing and reconfigurable logic devices. By providing a clear, reliable symbol, LTSpice facilitates accurate circuit modeling, aiding engineers and researchers in developing efficient memristor-based systems. The symbol's visual simplicity improves connectivity verification and streamlines simulation processes in hybrid and memory-focused designs.

Fig. Hystersis Curve of Memristor Model in LTSpice XVII

The image illustrates the hysteresis curve of a memristor model simulated in LTSpice XVII, showcasing its current-voltage (I-V) characteristics. In this graph, voltage (V) is plotted on the x-axis and current (I) on the y-axis. The curve features a distinct pinched hysteresis loop, a defining trait of memristors, demonstrating their memory effect where resistance varies based on the history of applied voltage and current.

The pinched loop at the origin highlights a key property of memristors — both current and voltage simultaneously reach zero. This characteristic is crucial for non-volatile memory applications, as the memristor retains its resistance state even when power is removed. The symmetric linear region in the curve reflects balanced behavior during both positive and negative voltage cycles.

The decreasing width of the hysteresis loop as voltage reduces indicates the memristor's transition from a high-conductance to a low-conductance state. This dynamic resistance change is essential for applications requiring precise conductance control. The area enclosed by the loop represents energy dissipation; a larger loop suggests higher dissipation, while a narrower loop indicates lower energy loss.

The slope of the curve at various points reflects the memristor's conductance — steeper slopes indicate lower resistance, while flatter slopes signify higher resistance. This adaptive behavior allows memristors to function effectively in circuits where resistance modulation is crucial.

In addition to memory storage applications, the memristor's hysteresis behavior is valuable in neuromorphic computing. Its ability to adjust resistance based on past voltage patterns mimics synaptic plasticity in biological systems, making it ideal for hardware designed for artificial intelligence and machine learning. LTSpice's accurate simulation of this behavior enables researchers to explore advanced circuit designs for emerging technologies such as ReRAM, adaptive systems, and next-generation computing architectures.

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V. CONCLUSION

The design and implementation of the memristor in LTSpice XVII have successfully demonstrated the fundamental characteristics of memristive behavior through simulation. The hysteresis curve obtained from the simulation clearly shows the voltage-current relationship, emphasizing the memristor's ability to exhibit a pinched hysteresis loop, which is a distinctive property of memristive devices. The observed linearity and symmetric response to positive and negative voltage swings validate the theoretical characteristics of memristors and highlight their potential for memory-based applications. Furthermore, the accurate representation of the memristor symbol in LTSpice XVII has enabled seamless integration into various circuit designs, promoting ease of simulation and ensuring the correct depiction of memristive properties. This reliable and accurate modeling offers a robust foundation for further research and development in memristive circuits, including applications in neuromorphic computing, memory devices, and reconfigurable logic circuits. As memristor technology continues to evolve, the simulation practices established in this study provide valuable insights into optimizing device performance and integration within complex electronic systems.

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